

MODEL NAME : *ZAU70*
PCB NO : *LA-B331P (DAA0008K010)*
BOM P/N :

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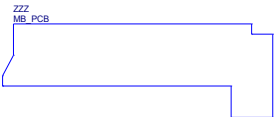
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Schematic Document

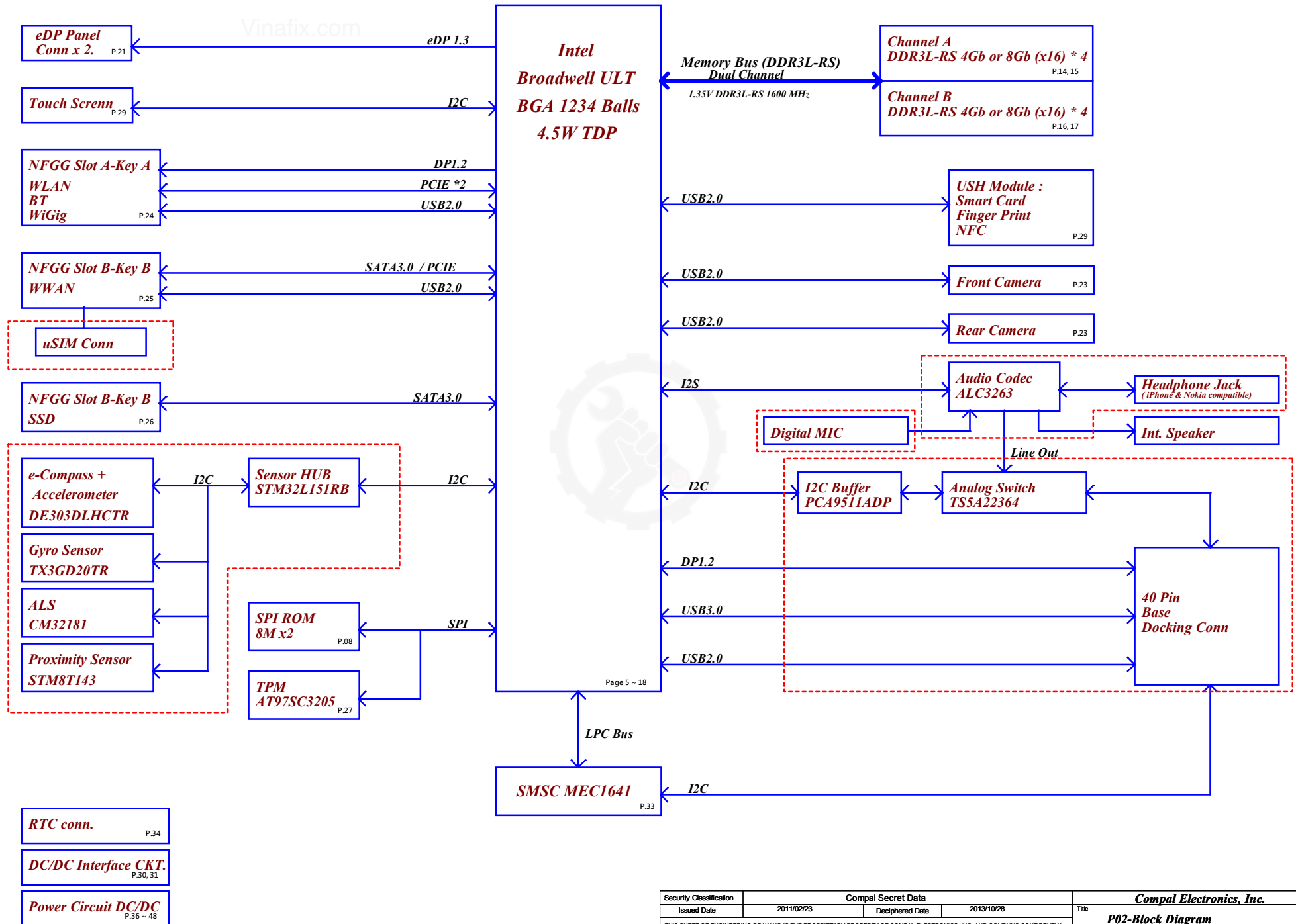
Crested Butte (Broadwell Y)

2014-08-13

Rev: 1.0



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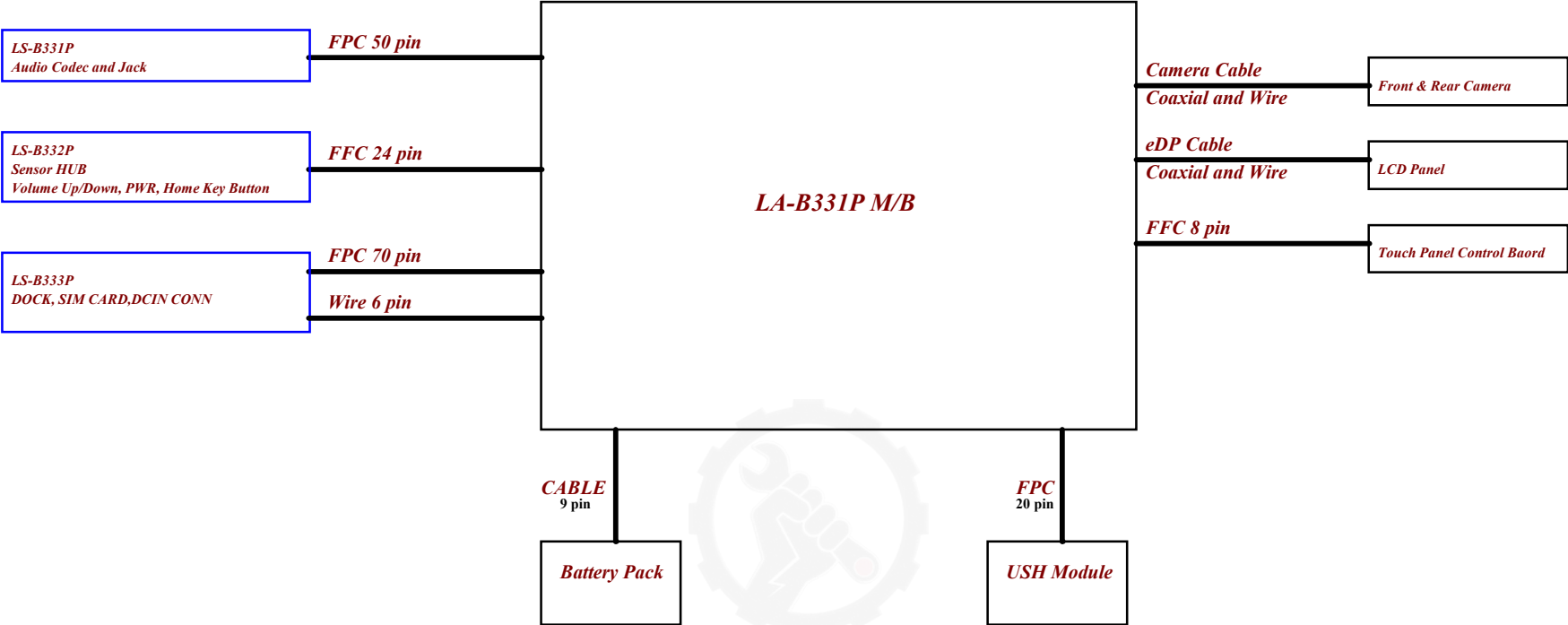


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Project Code : ZAU70

File Name : LA-B331P

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2011/06/02		2013/10/28		P03-DaughterB block diagram		
Size		Document Number		Rev		
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0.155 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V
2	18K +/- 5%	0.375 V	0.503 V	0.621 V
3	33K +/- 5%	0.634 V	0.819 V	0.945 V
4	56K +/- 5%	0.958 V	1.185 V	1.359 V
5	100K +/- 5%	1.372 V	1.650 V	1.838 V
6	200K +/- 5%	1.851 V	2.200 V	2.420 V
7	NC	2.433 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	Base
	1	Debug Port
	2	Front Camera
	3	
	4	Rear Camera
	5	NGFF (WWAN)
	6	NGFF (WLAN)
	7	USH

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	Base (mini-DP)
	C	NGFF (WiGig)

SMBUS Control Table

	SOURCE	Base	BATT	Charger	USH	XDP
PCH_SMLCLK PCH_SMLDATA	PCH					
PCH_SML1CLK PCH_SML1DATA	PCH					
MEM_SMBCLK MEM_SMBDATA	PCH					V
EC_SMB00_CLK EC_SMB00_DAT	MEC1641					
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V	
EC_SMB03_CLK EC_SMB03_DAT	MEC1641		V			
EC_SMB04_CLK EC_SMB04_DAT	MEC1641			V		
EC_SMB05_CLK EC_SMB05_DAT	MEC1641	V				

Link

USB 3.0 PORT#	DESTINATION
1	Base
2	
3	
4	



SATA	DESTINATION
SATA0	
SATA1	NGFF SSD
SATA2	
SATA3	NGFF (WWAN)

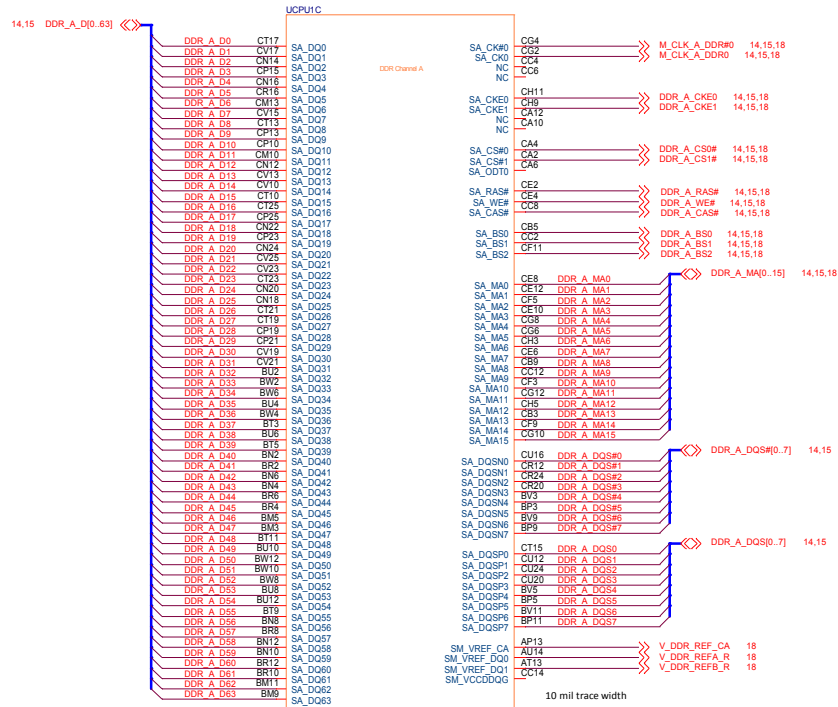
CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	
	CLKOUT_PCIE1	
	CLKOUT_PCIE2	NGFF (WLAN)
	CLKOUT_PCIE3	
	CLKOUT_PCIE4	NGFF (WLAN)
	CLKOUT_PCIE5	NGFF (WWAN)

PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF (WLAN)
Lane 4	
Lane 5	NGFF (WLAN)
Lane 6	NGFF (WWAN)

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	Debug

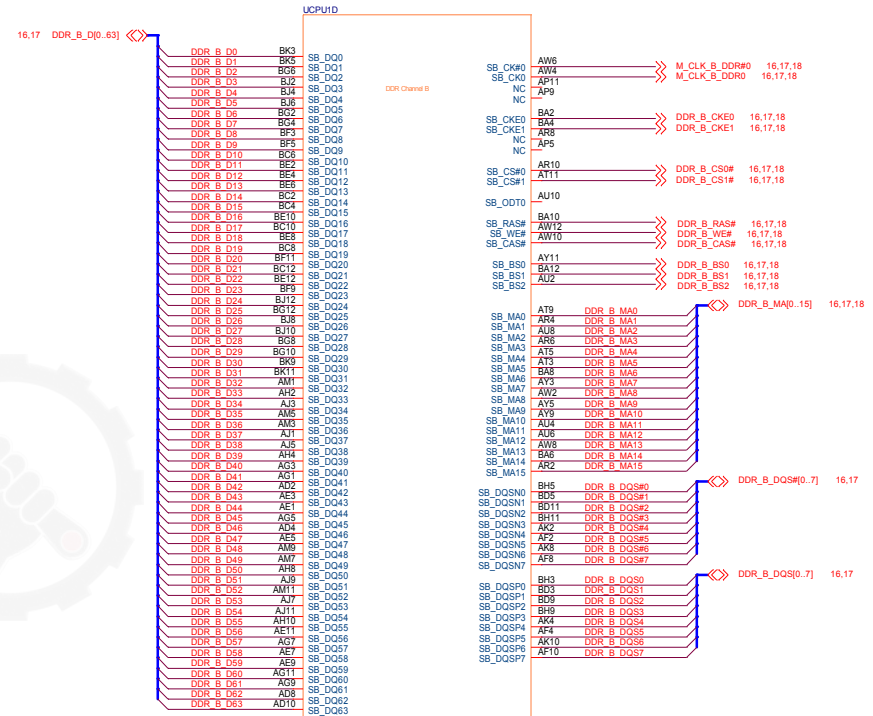
Symbol Note :

 : means Digital Ground
 : means Analog Ground



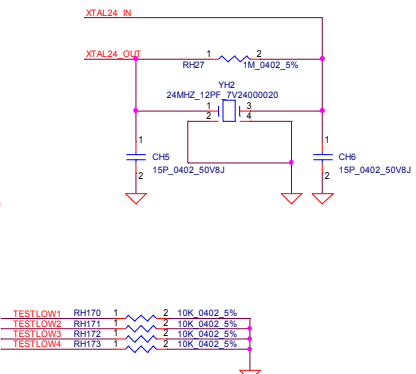
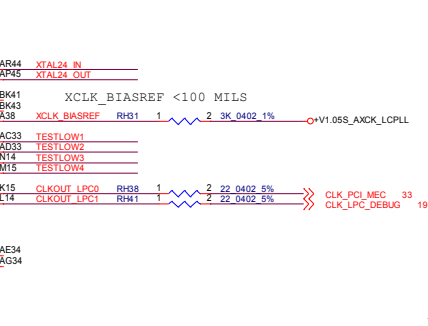
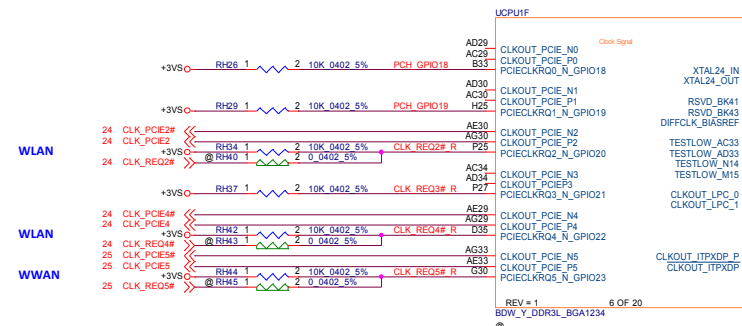
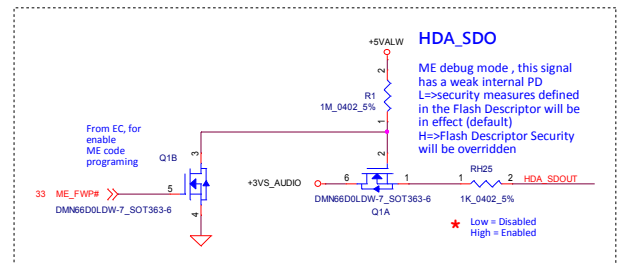
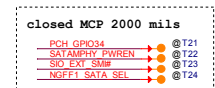
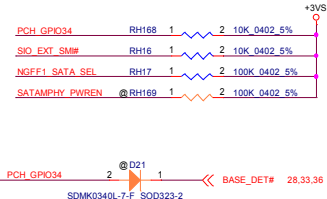
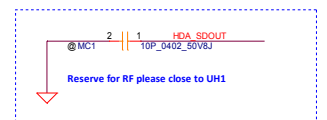
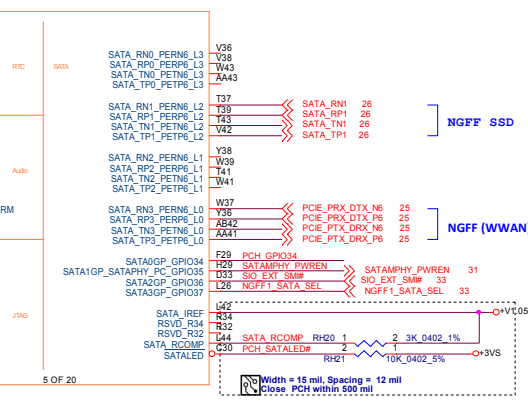
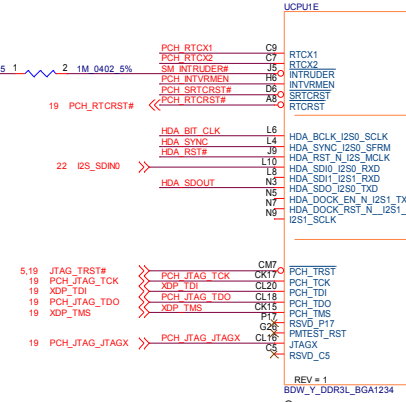
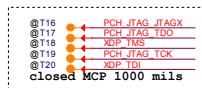
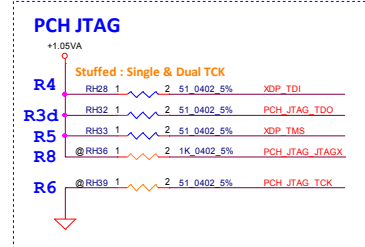
REV = 1 3 OF 20
BDW_Y_DDR3L_BGA1234

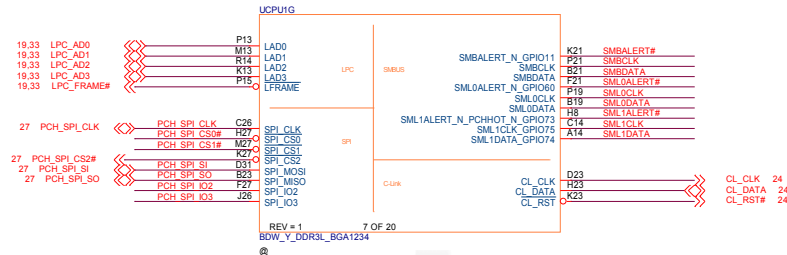
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REV = 1 4 OF 20
DOWN X DDD2L DCA1234

BDW_Y_DDR3L_BGA1234

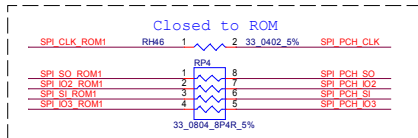
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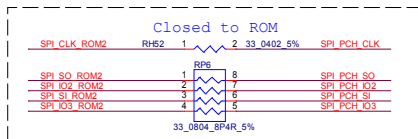
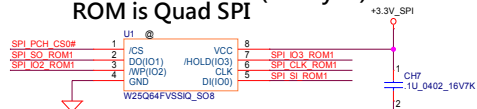


SML1CLK @ RH55 1 2 0 0402 5% SML1_SMBCLK 33
SML1DATA @ RH56 1 2 0 0402 5% SML1_SMBDATA 33

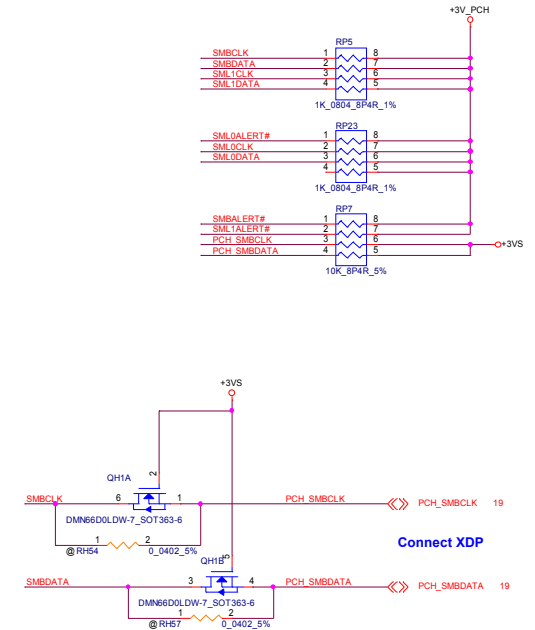
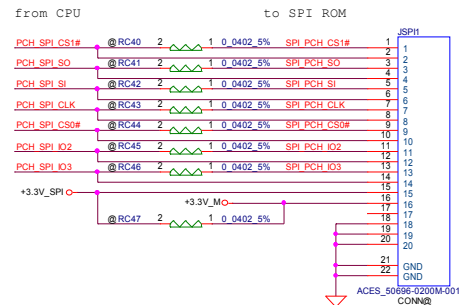
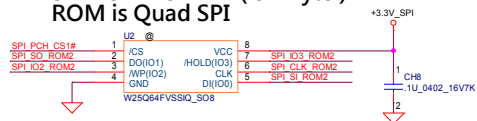
Connect EC



SPI ROM FOR ME (8MByte) ROM is Quad SPI

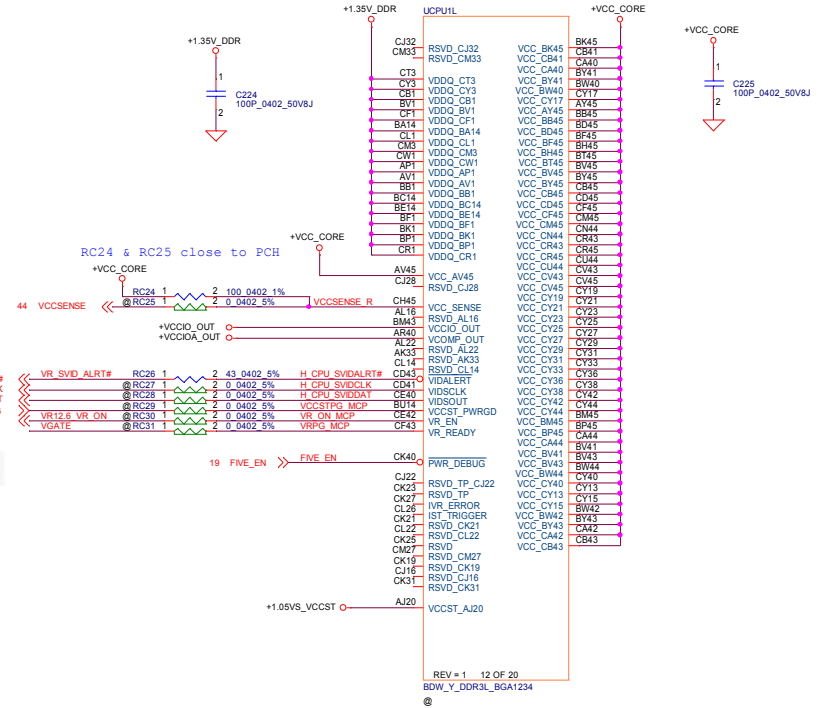
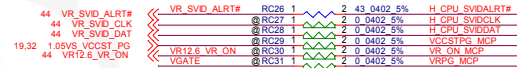
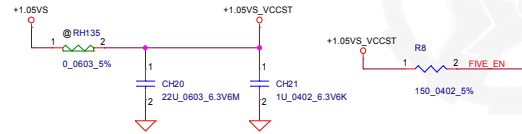
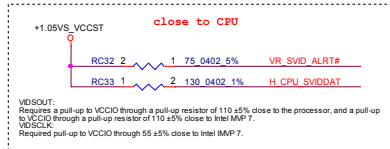
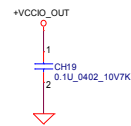
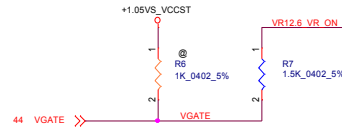
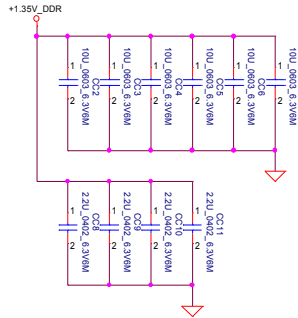
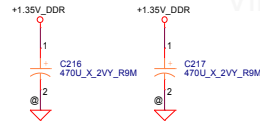


SPI ROM FOR ME (8MByte) ROM is Quad SPI



Connect XDP

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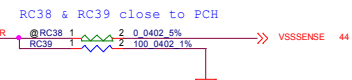
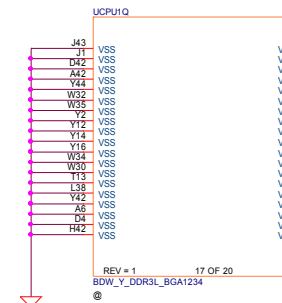
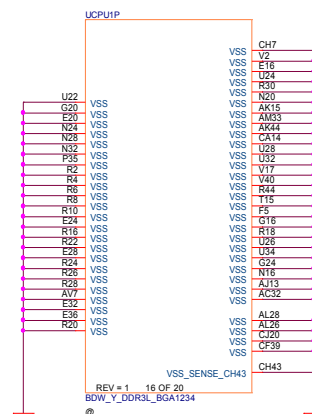
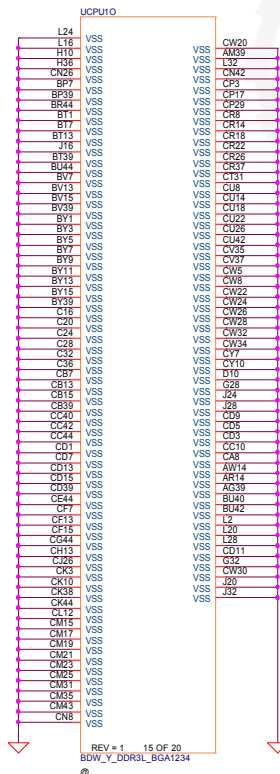
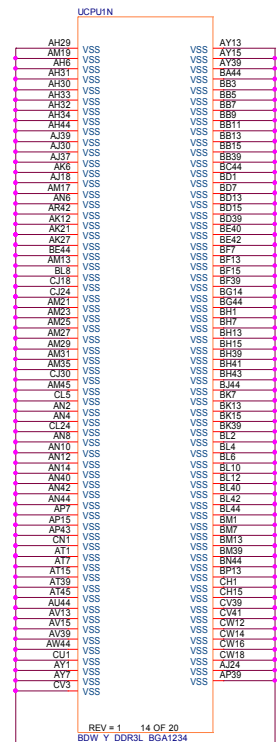
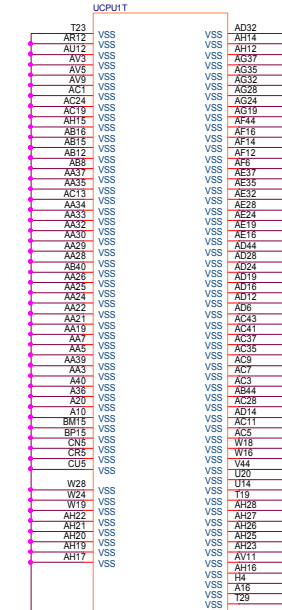
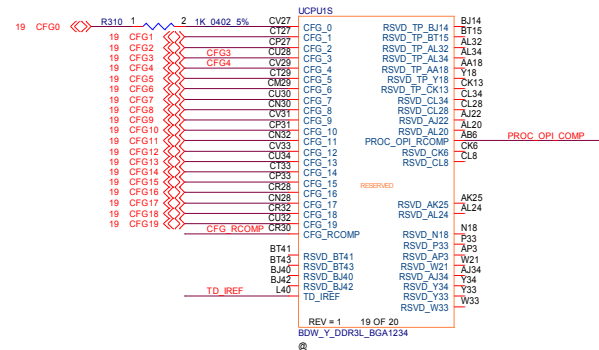
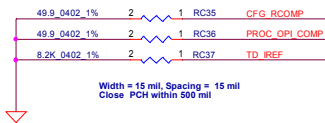
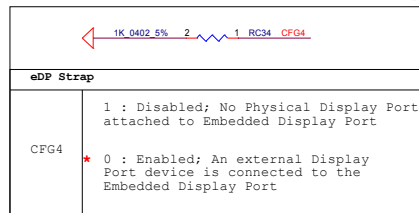


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BDW_Y_DOR3L_BGA1234

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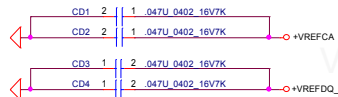
DCPSUS can be NC, if INTVRMEN pull up to enable integrated VRM

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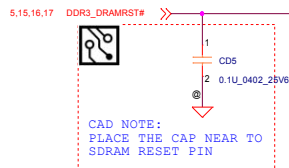
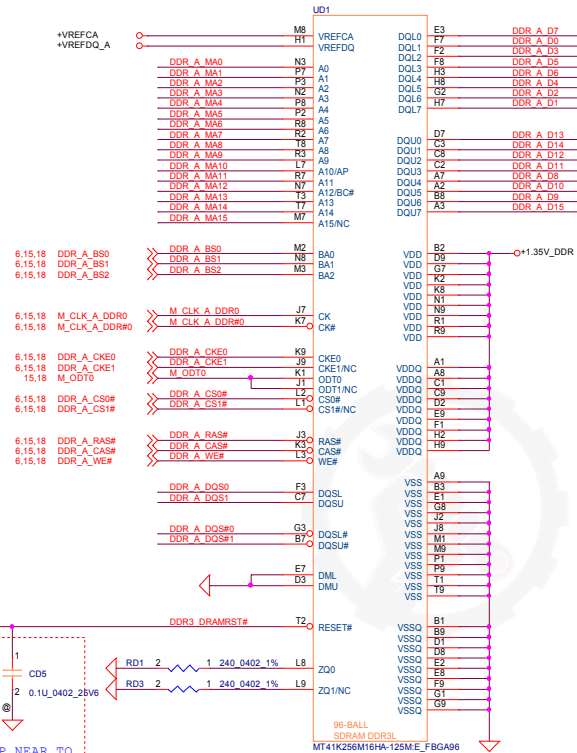


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

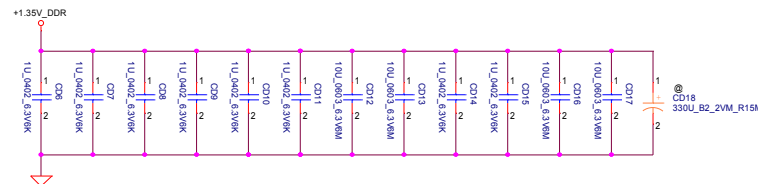


6.15 DDR_A_DQS[0..7] <>>
6.15 DDR_A_DQS[0..7] <>>
6.15 DDR_A_D[0..63] <>>
6.15.18 DDR_A_MA[0..15] <>>

All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



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						Size		Document Number		Rev	
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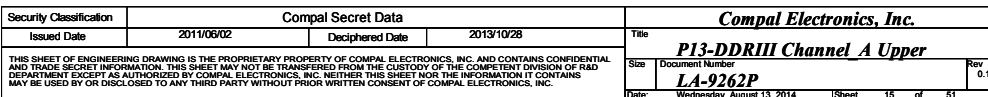
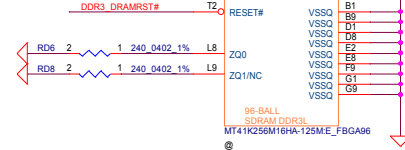
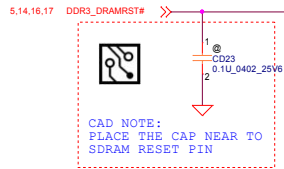
CD19_2 1 .047U_0402_16V7K
CD20_2 1 .047U_0402_16V7K
+VREFCA

CD21_1 2 .047U_0402_16V7K
CD22_1 2 .047U_0402_16V7K
+VREFDO_A

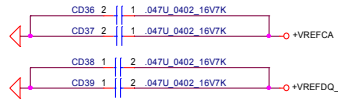
**PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS**



6,14	DDR_A_DQS#[0..7]	⏏	
6,14	DDR_A_DQS[0..7]	⏏	
6,14	DDR_A_D[0..63]	⏏	
6,14,18	DDR_A_MA[0..15]	⏏	



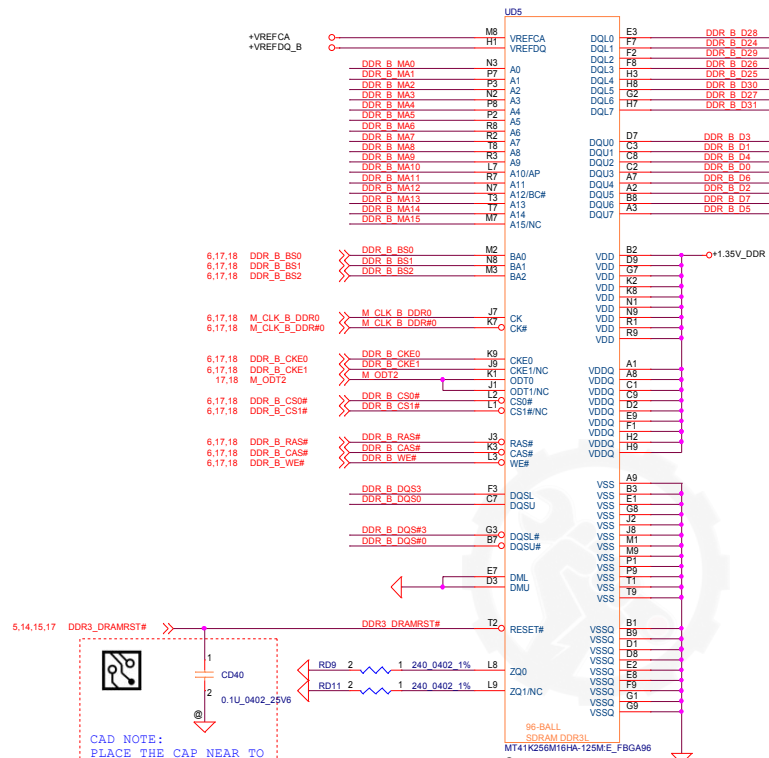
follow INTEL PDG



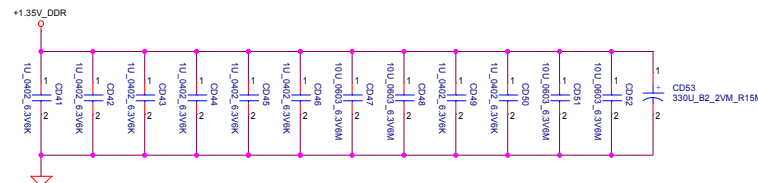
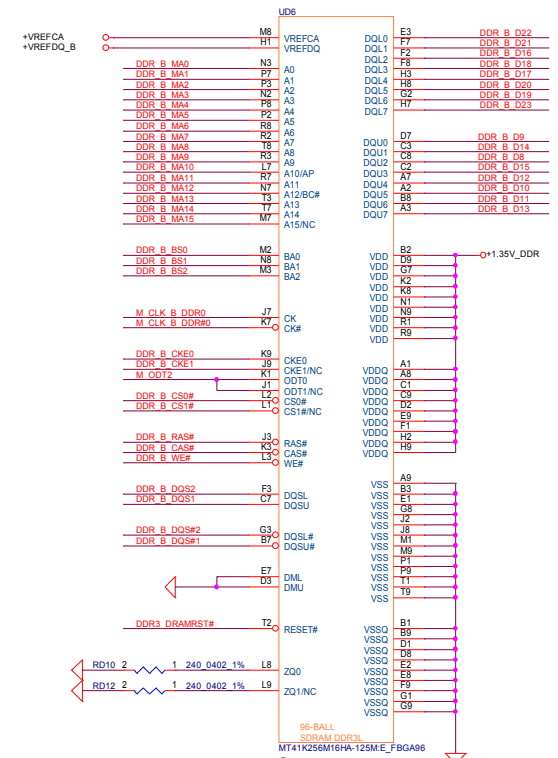
PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS



All VREF traces should
have 10 mil trace width

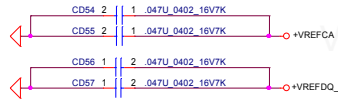


CAD NOTE:
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SDRAM RESET PIN



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							51

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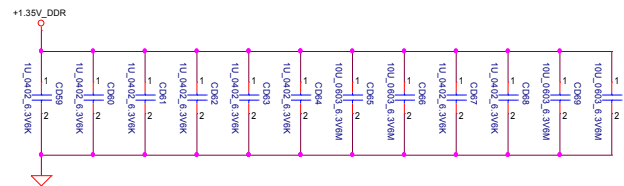
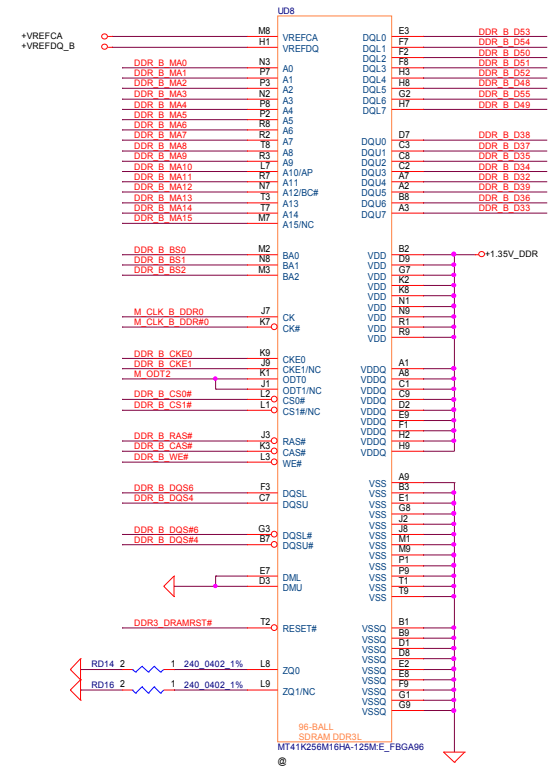
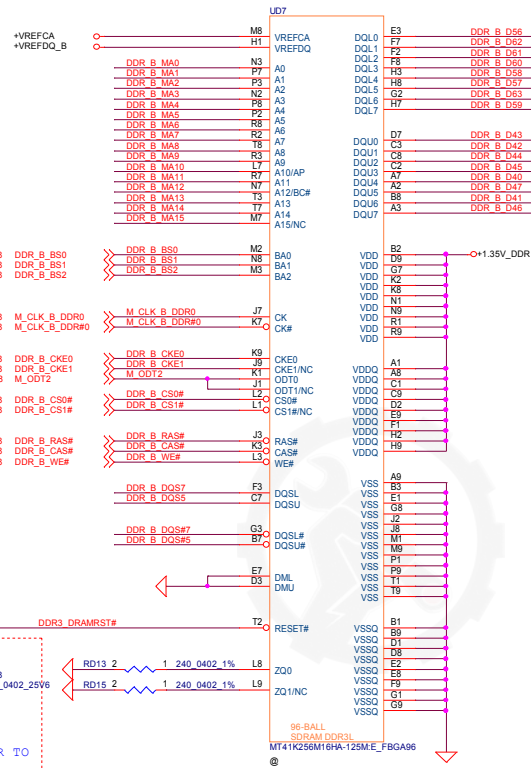


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS



6.16 DDR_B_DQS#0..7] <<>>
6.16 DDR_B_DQS#0..7] <<>>
6.16 DDR_B_DQS#0..7] <<>>
6.16.18 DDR_B_MA[0..15] <<>>

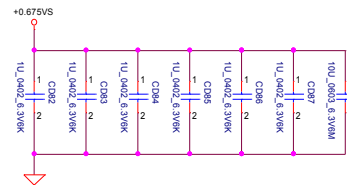
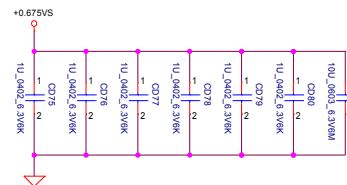
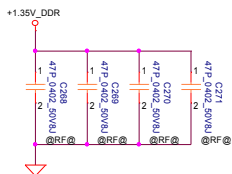
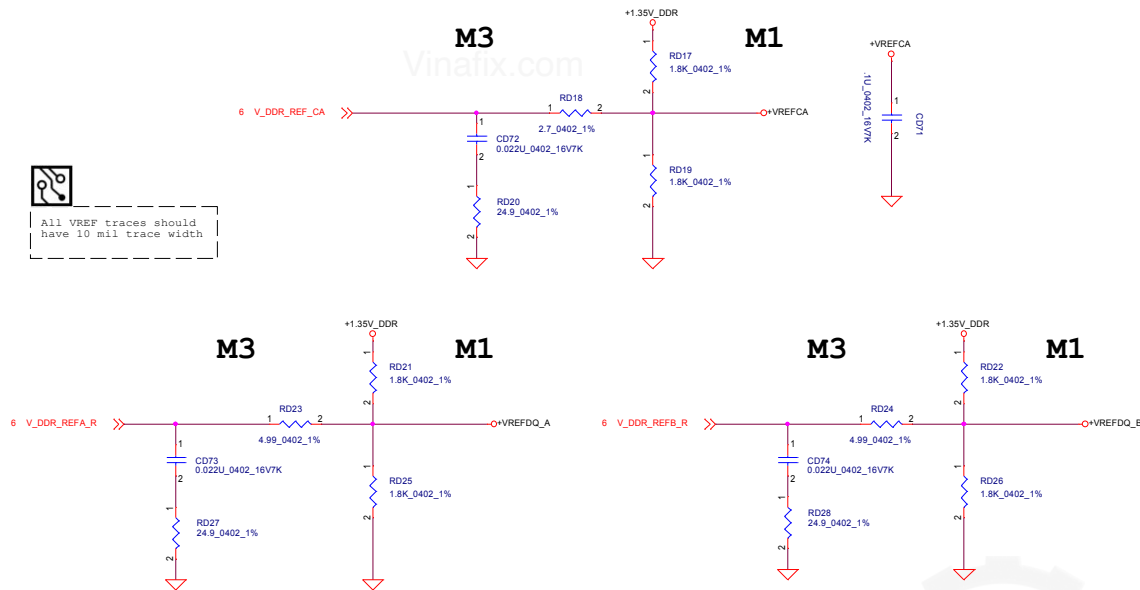
All VREF traces should
have 10 mil trace width





All VREF traces should have 10 mil trace width

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DDR A MA12 RD29 1 2 34.8 0402 1%
DDR A MA15 RD31 1 2 34.8 0402 1%
DDR A MA9 RD33 1 2 34.8 0402 1%
DDR A MA10 RD35 1 2 34.8 0402 1%

DDR A MA4 RD37 1 2 34.8 0402 1%
DDR A MA2 RD39 1 2 34.8 0402 1%
DDR A MA1 RD41 1 2 34.8 0402 1%
DDR A MA6 RD43 1 2 34.8 0402 1%

DDR A MA3 RD45 1 2 34.8 0402 1%
DDR A MA9 RD47 1 2 34.8 0402 1%
DDR A MA11 RD49 1 2 34.8 0402 1%
DDR A MA5 RD51 1 2 34.8 0402 1%

DDR A MA14 RD53 1 2 34.8 0402 1%
DDR A MA7 RD55 1 2 34.8 0402 1%
DDR A MA8 RD57 1 2 34.8 0402 1%
DDR A MA13 RD59 1 2 34.8 0402 1%

DDR A_CKE0 RD61 1 2 34.8 0402 1%
DDR A_RAS# RD63 1 2 34.8 0402 1%
DDR A_CS# RD65 1 2 34.8 0402 1%
DDR A_CAS# RD67 1 2 34.8 0402 1%

DDR A_WE# RD69 1 2 34.8 0402 1%
DDR A_BS0 RD71 1 2 34.8 0402 1%
DDR A_BS2 RD73 1 2 34.8 0402 1%
DDR A_BS1 RD75 1 2 34.8 0402 1%

DDR A_CKE1 RD77 1 2 34.8 0402 1%
DDR A_CS1# RD79 1 2 34.8 0402 1%

M_ODT0 RD81 1 2 30 0402 1%

M_CLK_A_DDR0 RD83 1 2 26.1 0402 1%

M_CLK_A_DDR# RD85 1 2 26.1 0402 1%

DDR B MA12 RD30 1 2 34.8 0402 1%
DDR B MA15 RD32 1 2 34.8 0402 1%
DDR B MA9 RD34 1 2 34.8 0402 1%
DDR B MA10 RD36 1 2 34.8 0402 1%

DDR B MA14 RD38 1 2 34.8 0402 1%
DDR B MA6 RD40 1 2 34.8 0402 1%
DDR B MA4 RD42 1 2 34.8 0402 1%
DDR B MA2 RD44 1 2 34.8 0402 1%

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DDR B MA1 RD48 1 2 34.8 0402 1%
DDR B MA13 RD50 1 2 34.8 0402 1%
DDR B MA7 RD52 1 2 34.8 0402 1%

DDR B MA3 RD54 1 2 34.8 0402 1%
DDR B MA9 RD56 1 2 34.8 0402 1%
DDR B MA11 RD58 1 2 34.8 0402 1%
DDR B MA5 RD60 1 2 34.8 0402 1%

DDR B_CKE0 RD62 1 2 34.8 0402 1%
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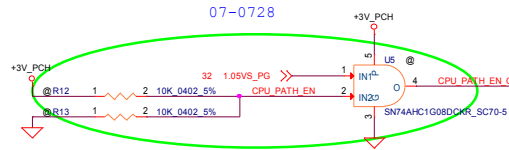
DDR B_WE# RD70 1 2 34.8 0402 1%
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DDR B_BS2 RD74 1 2 34.8 0402 1%
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DDR B_CKE1 RD78 1 2 34.8 0402 1%
DDR B_CS1# RD80 1 2 34.8 0402 1%

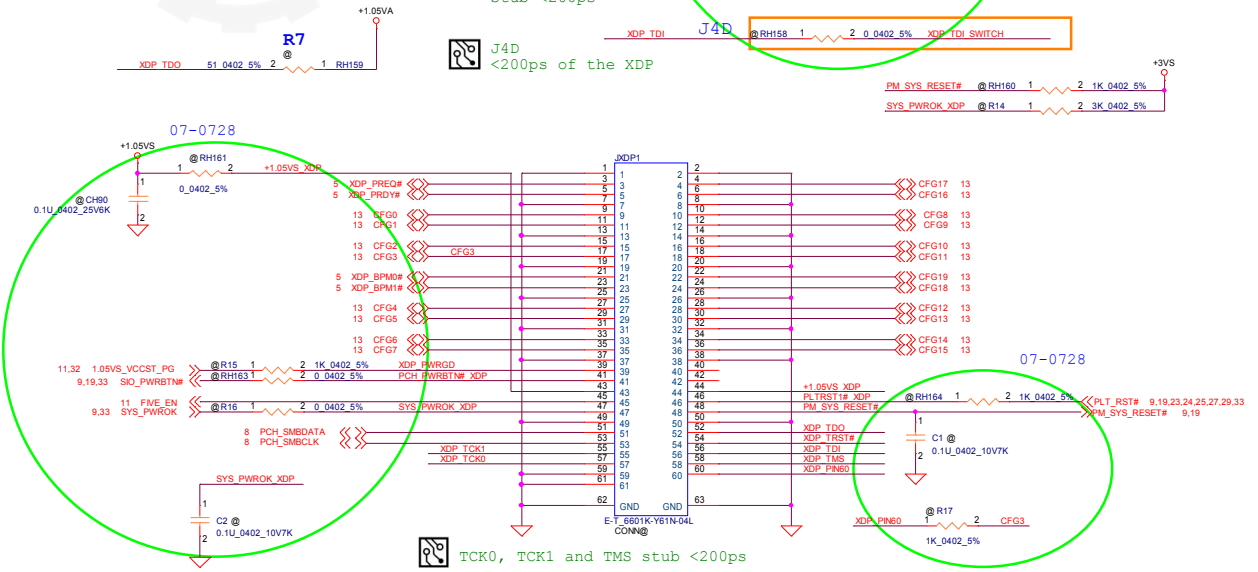
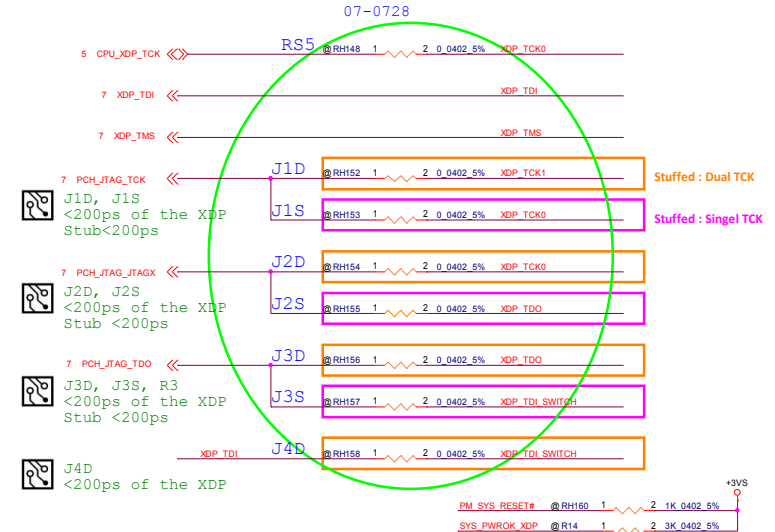
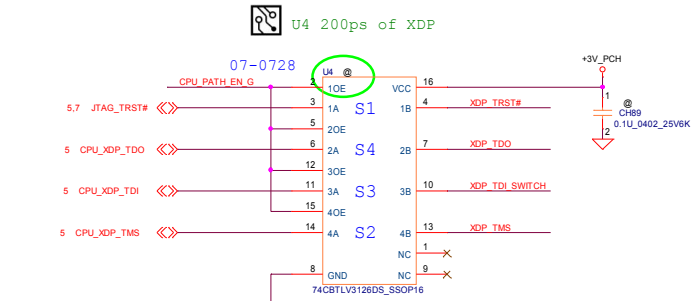
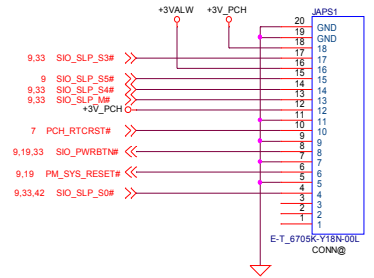
M_ODT2 RD82 1 2 30 0402 1%

M_CLK_B_DDR0 RD84 1 2 26.1 0402 1%

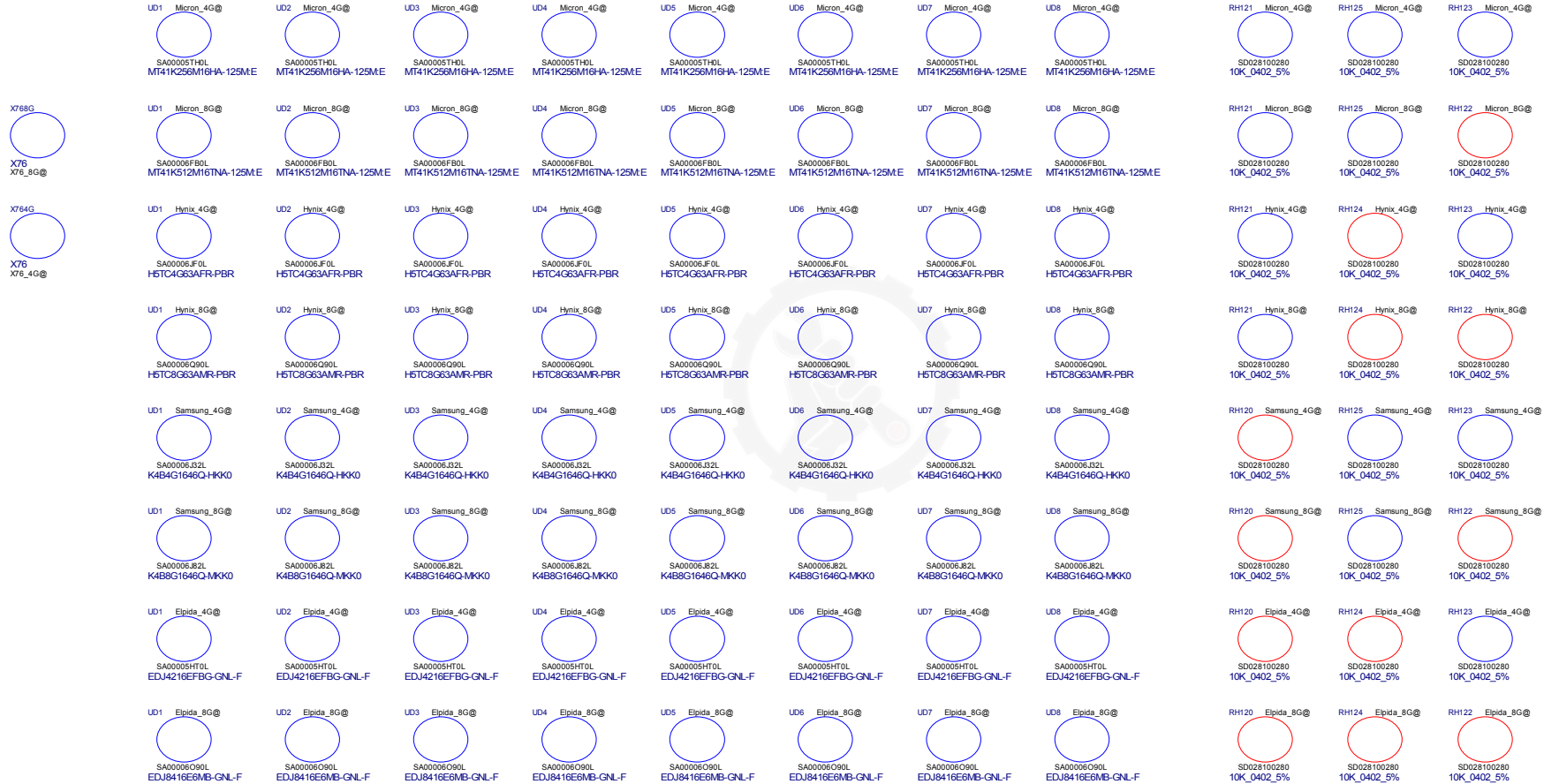
M_CLK_B_DDR# RD86 1 2 26.1 0402 1%

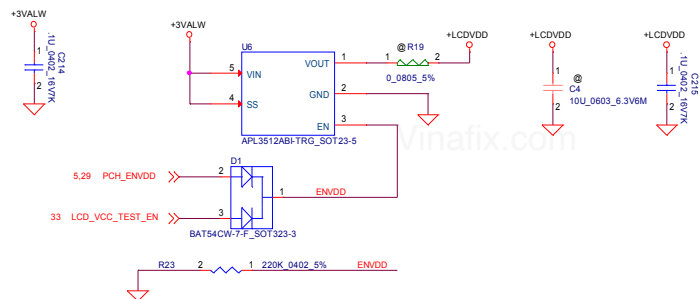


R7

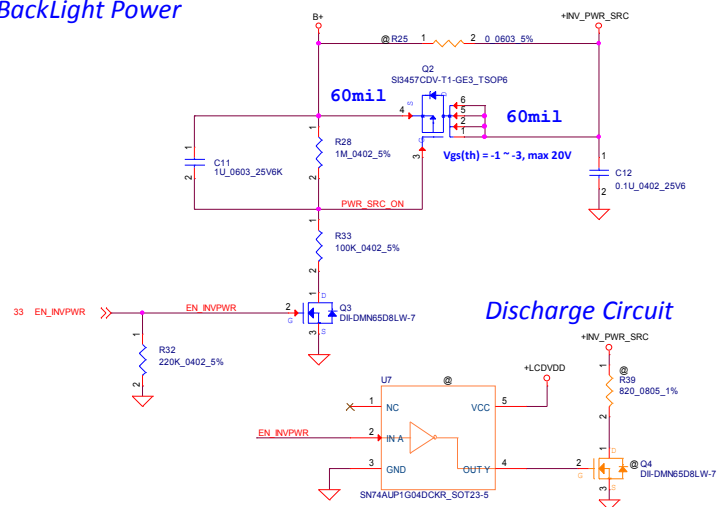


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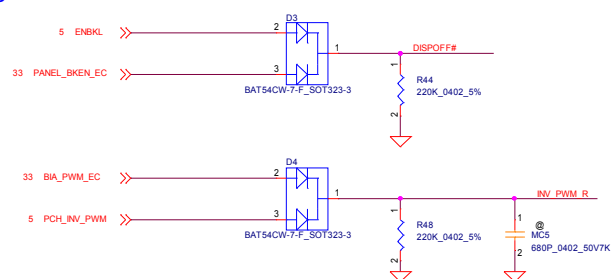




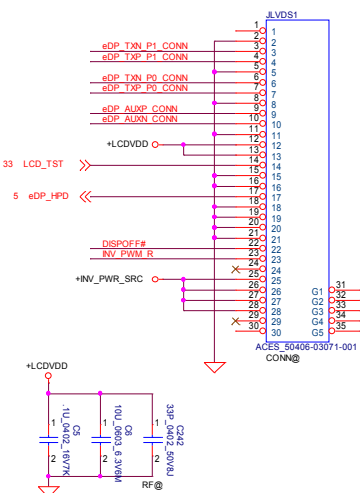
eDP BackLight Power



BackLight PWM Control



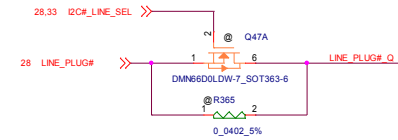
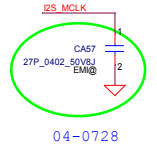
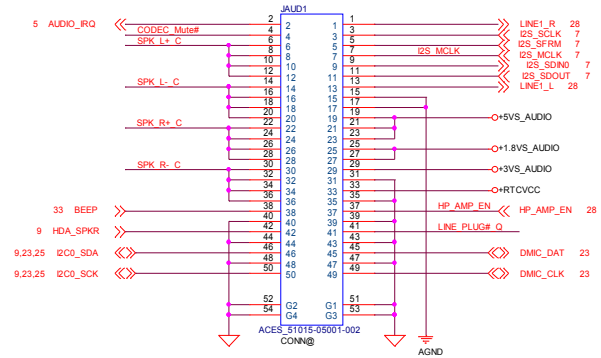
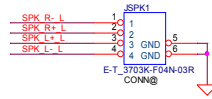
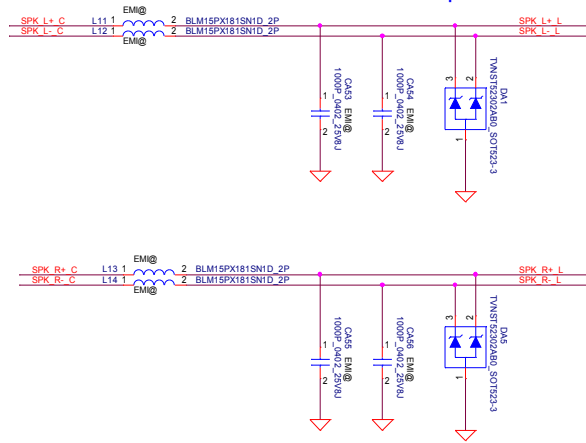
eDP Conn



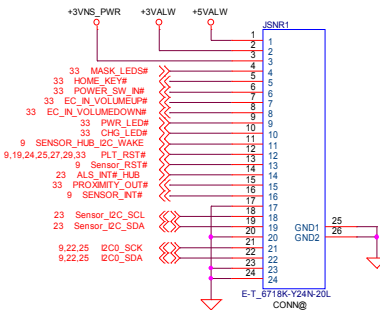
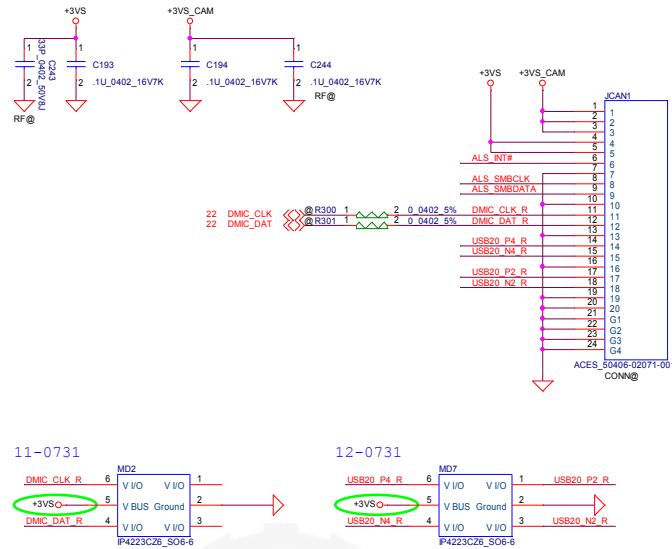
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Issued Date	2011/05/02	Deciphered Date	2013/10/28	Title	P17-eDP/ Camera CONN
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				Date:	Wednesday, August 13, 2014
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Int. Speaker Conn.

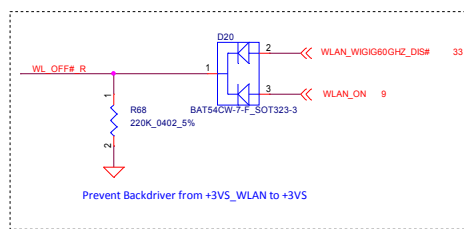
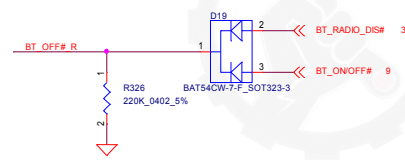
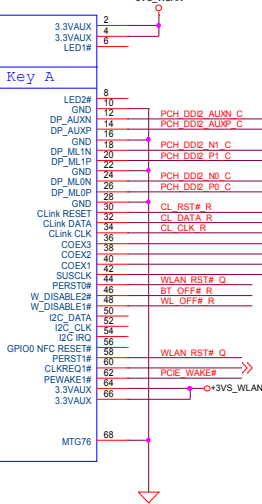
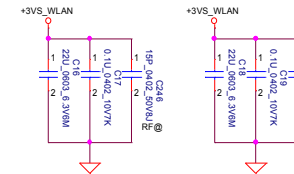
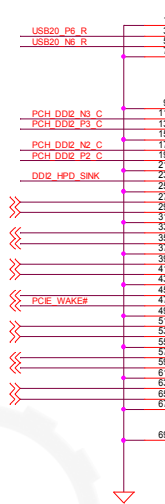
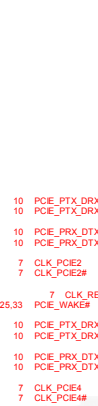
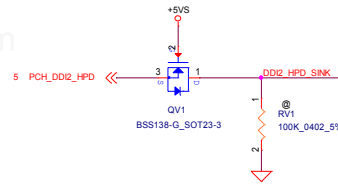
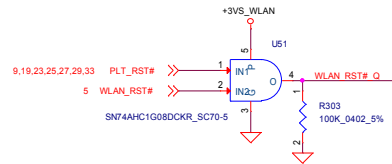
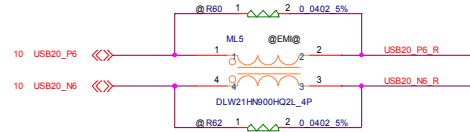
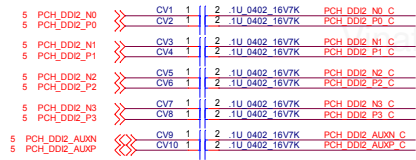
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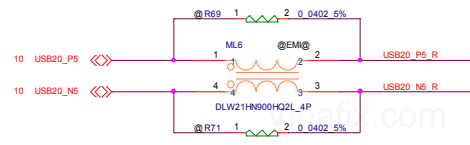


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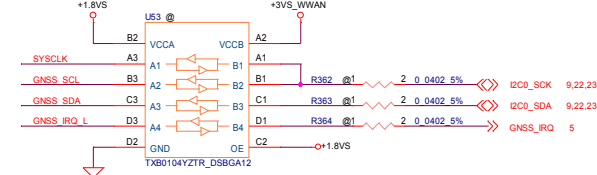
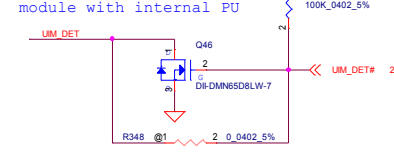
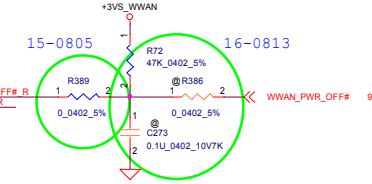
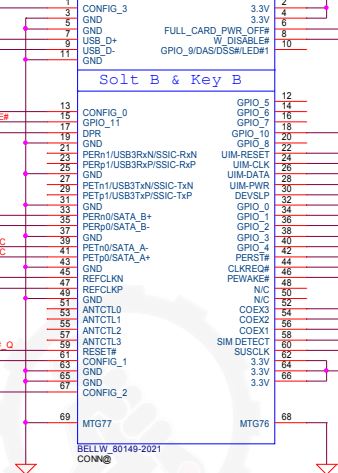
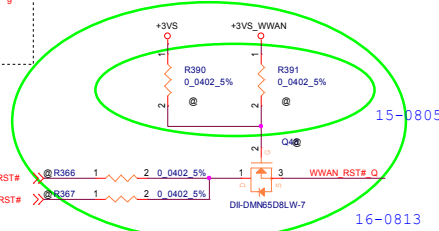
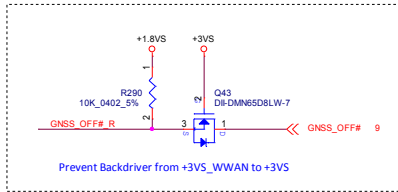
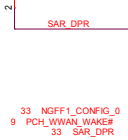
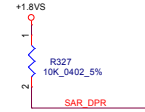
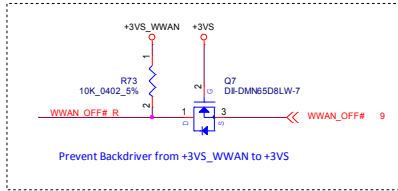
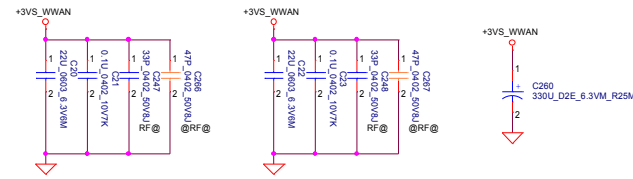


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				Size: Document Number LA-9262P	
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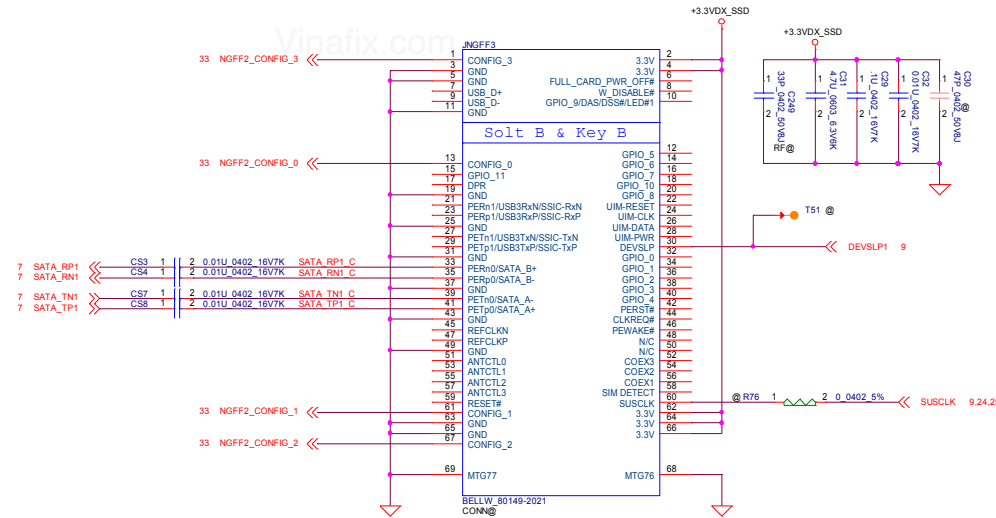
closed to pin 2, 4 closed to pin 64, 66

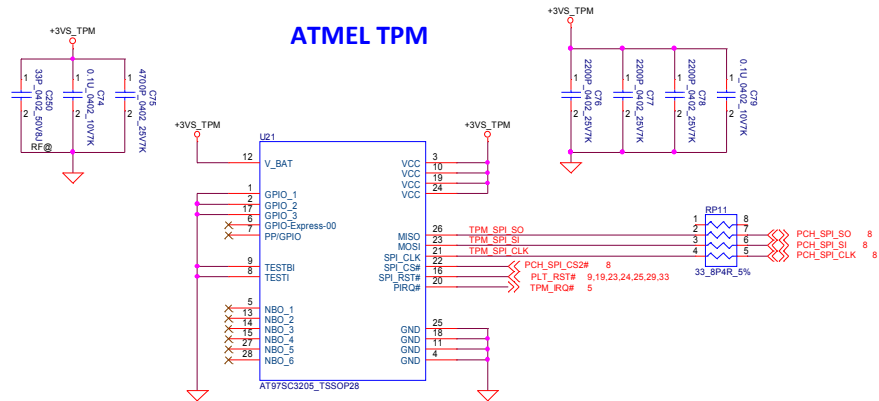


State#	CONFIG 0 (Pin 2I)	CONFIG 1 (Pin 69)	CONFIG 2 (Pin 75)	CONFIG 3 (Pin 1)	Module Type	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	GND	HIGH	GND	WWAN - PCIe	0
3	GND	HIGH	HIGH	GND	WWAN - PCIe	1
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1
10	HIGH	GND	HIGH	GND	WWAN - SSIC	2
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
12	HIGH	GND	GND	HIGH	WWAN - PCIe	2
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	3
14	HIGH	GND	HIGH	HIGH	DDP/HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A

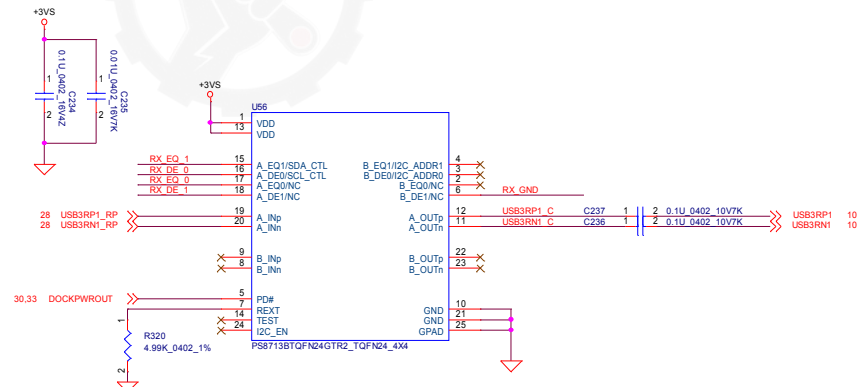
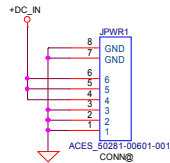
Pin	Port Config_0	Port Config_1	Port Config_2	Port Config_3
GPIO_0	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	GNSS_SDA	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	SYSClk	GNSS_0	UIM_RST2	IPC_3
GPIO_4	TX BLANKING	GNSS_1	UIM_PWR2	IPC_4
GPIO_5	AUDIO_0	AUDIO_0	RFU	AUDIO_0
GPIO_6	AUDIO_1	AUDIO_1	RFU	AUDIO_1
GPIO_7	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9	LED_1#	LED_1#	LED_1#	IPC_7
GPIO_10	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA

NGFF(SATA)

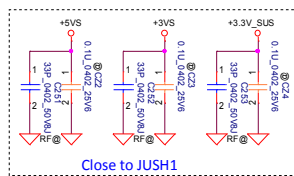
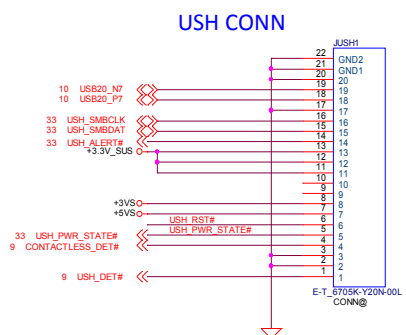
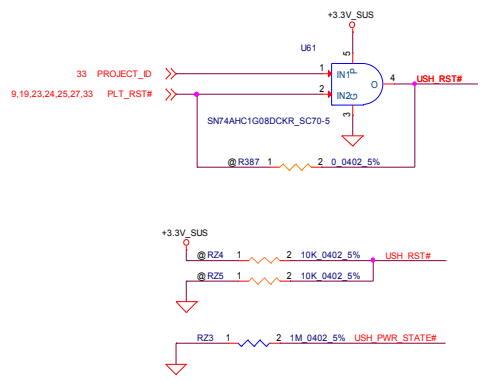
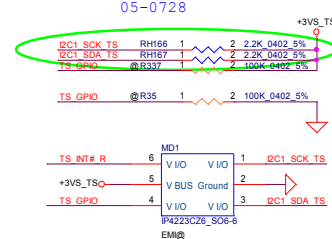
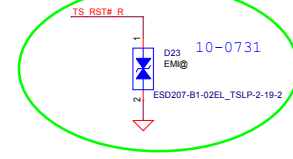
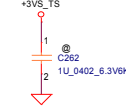
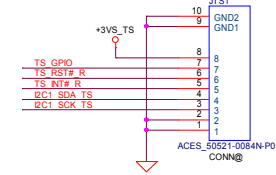
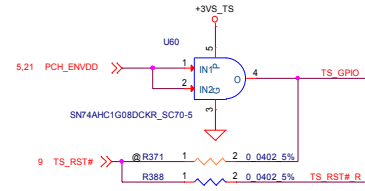
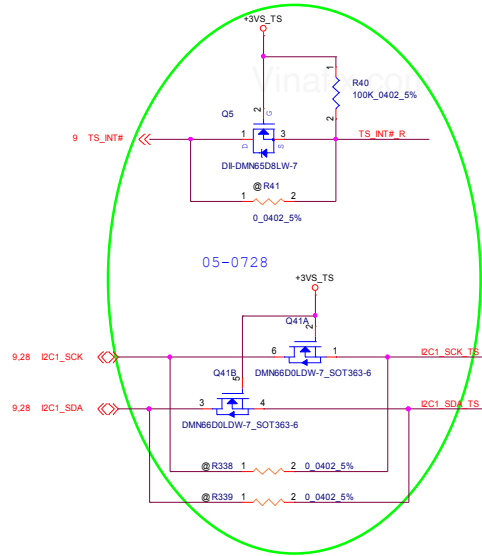




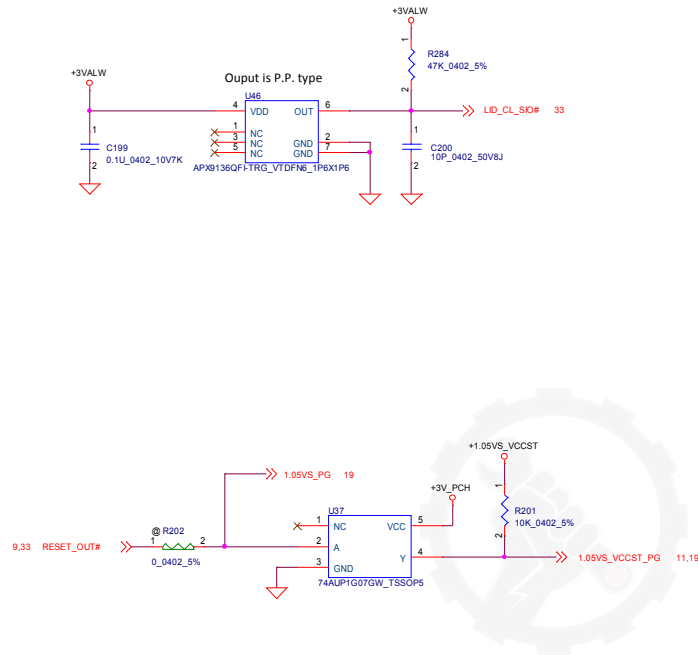
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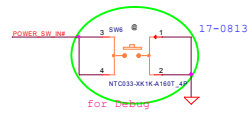
Rev	0.1
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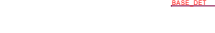
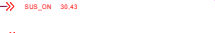
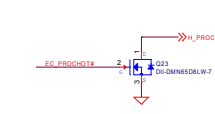
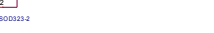
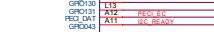
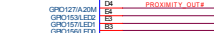
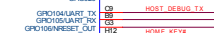
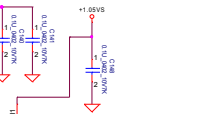
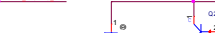
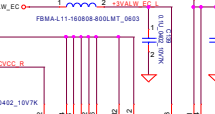
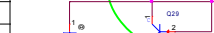
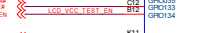
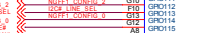
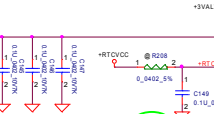
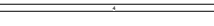
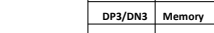
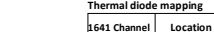
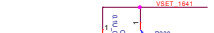
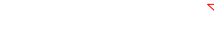
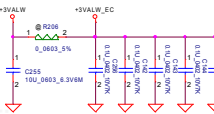
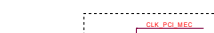
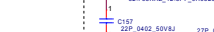
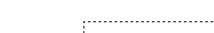
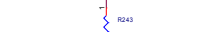
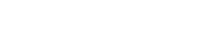
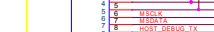
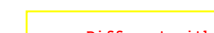
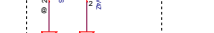
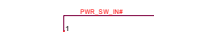
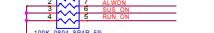
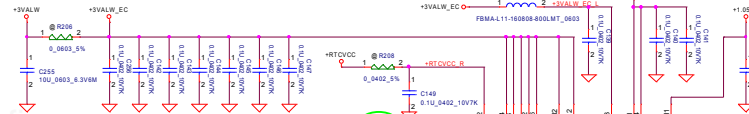
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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Size	C	Document Number	LA-A161P	Rev	0.1
Date: Wednesday, August 13, 2014		Sheet		29 of 51	

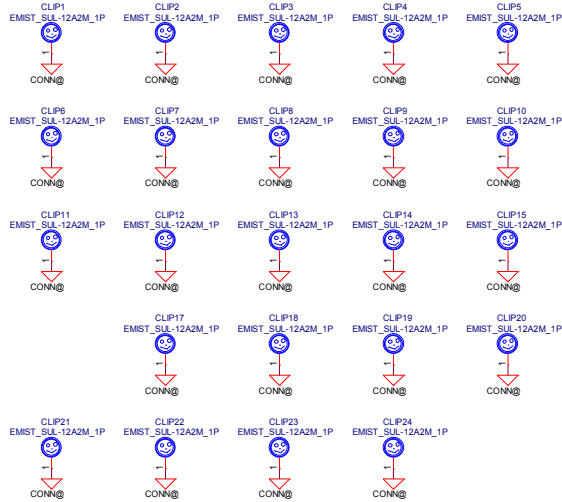
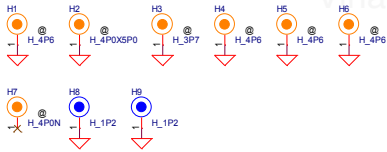
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				Date	Wednesday, August 13, 2014
				Sheet	32 of 51
				Rev	0.1

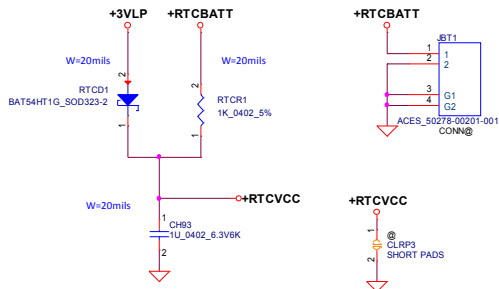


Vinafix.com

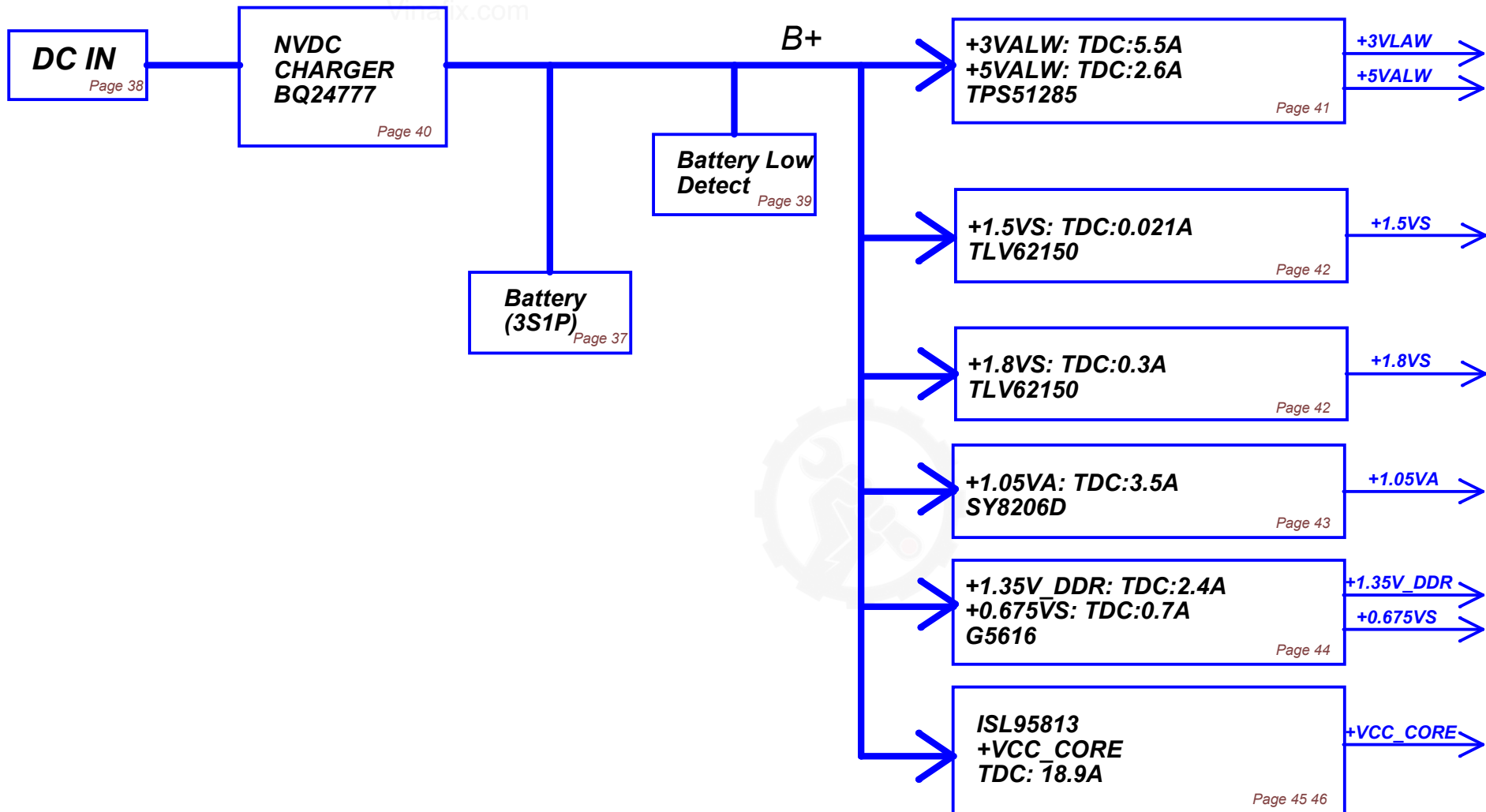




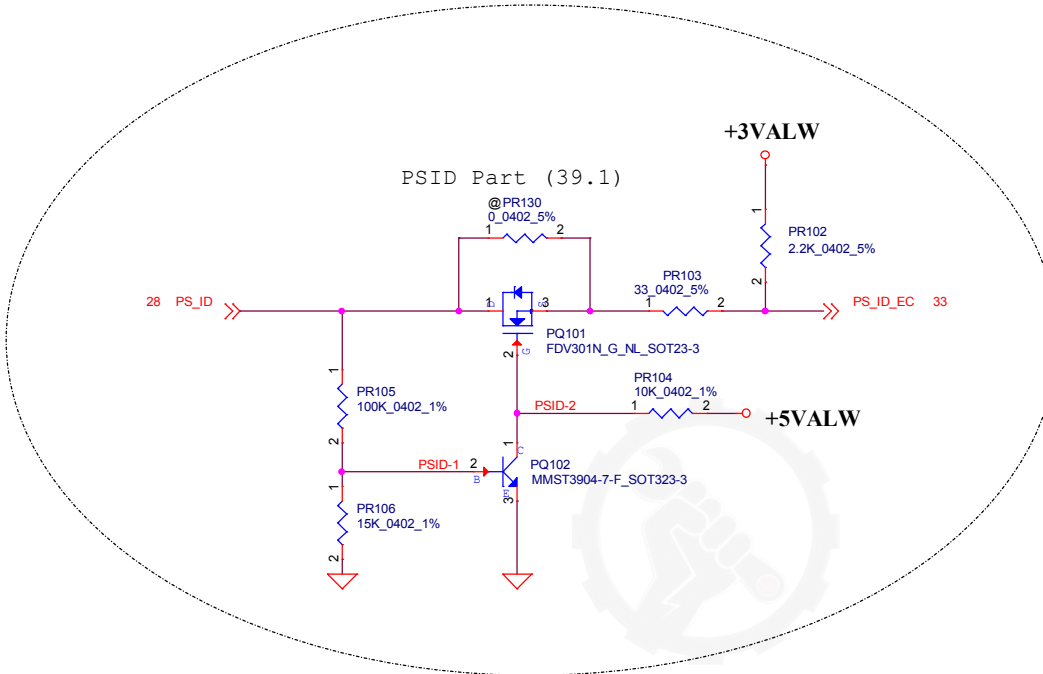
RTC Battery



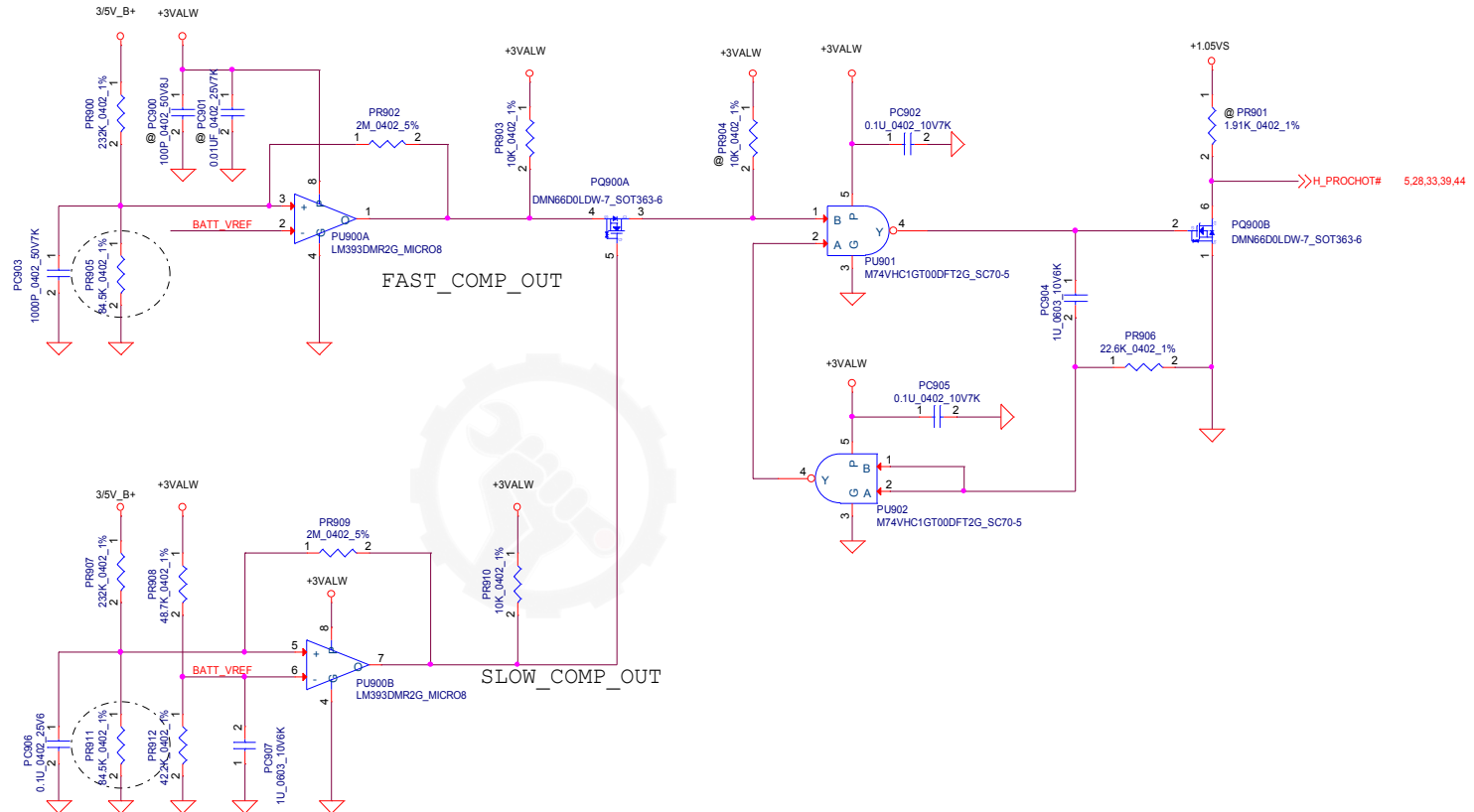
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Issued Date		Deciphered Date		Title	
2011/05/02		2013/10/28		P26-SCREWH/KB/RTC	
Size		Document Number		Rev	
LA-9262P		0.1		Date	
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P33-PWR Block Diagram
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				Date:	Wednesday, August 13, 2014
				Sheet	35 of 51
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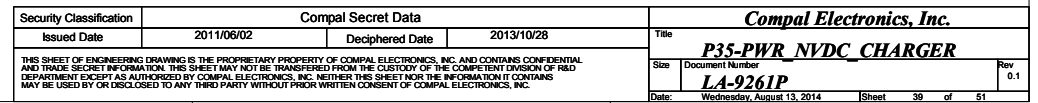


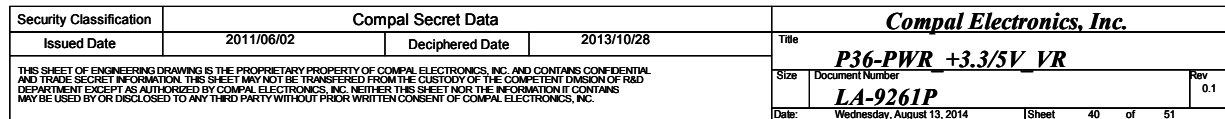
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Date: Wednesday, August 13, 2014		Sheet 37 of 51			

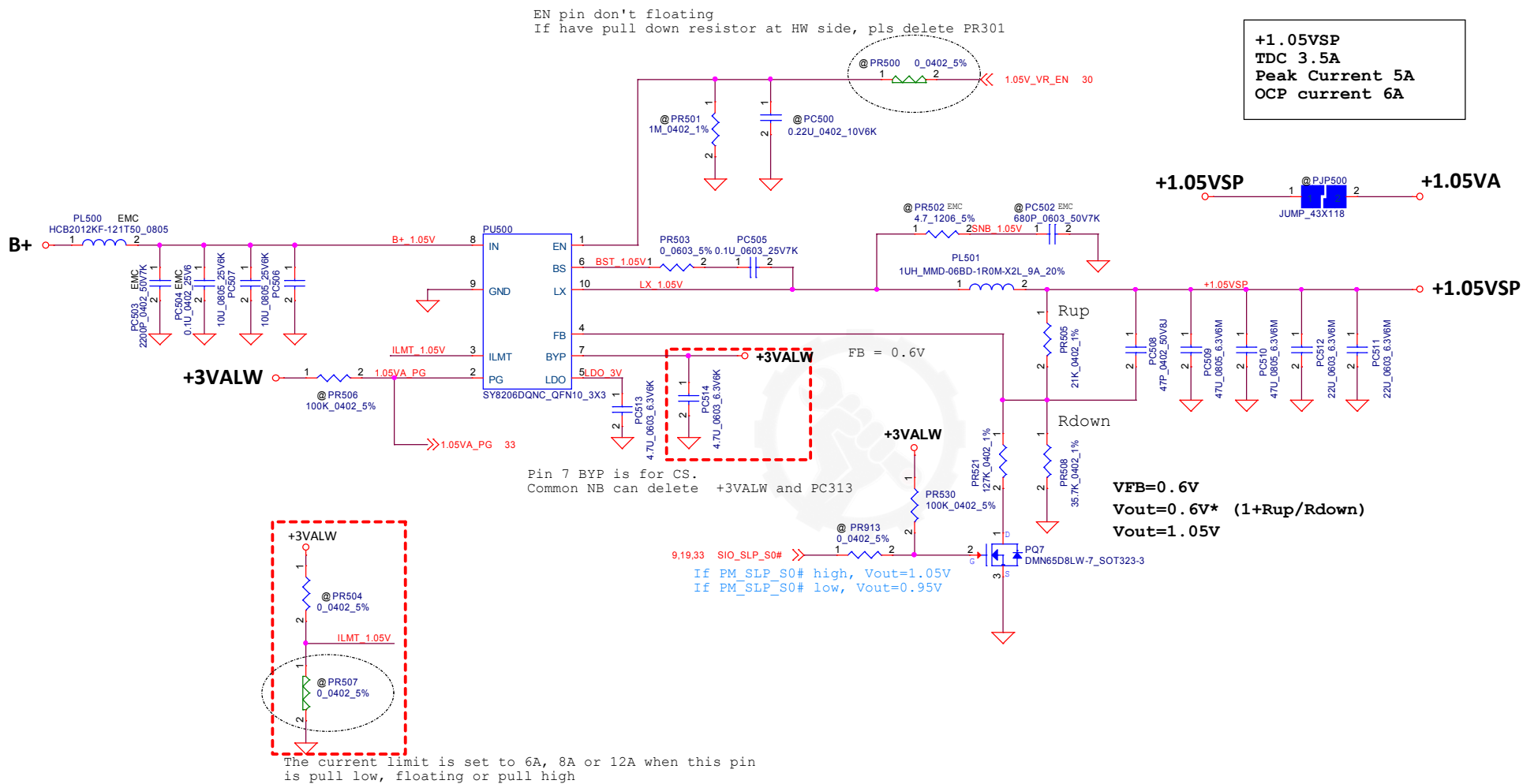


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				Date	Rev
				Wednesday, August 13, 2014	0.1
				Sheet	38 of 51

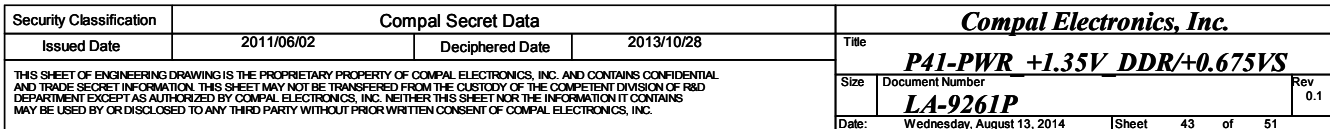
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Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +1.05VA	
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					LA-9261P	0.1
				Date:	Wednesday, August 13, 2014	Sheet 42 of 51

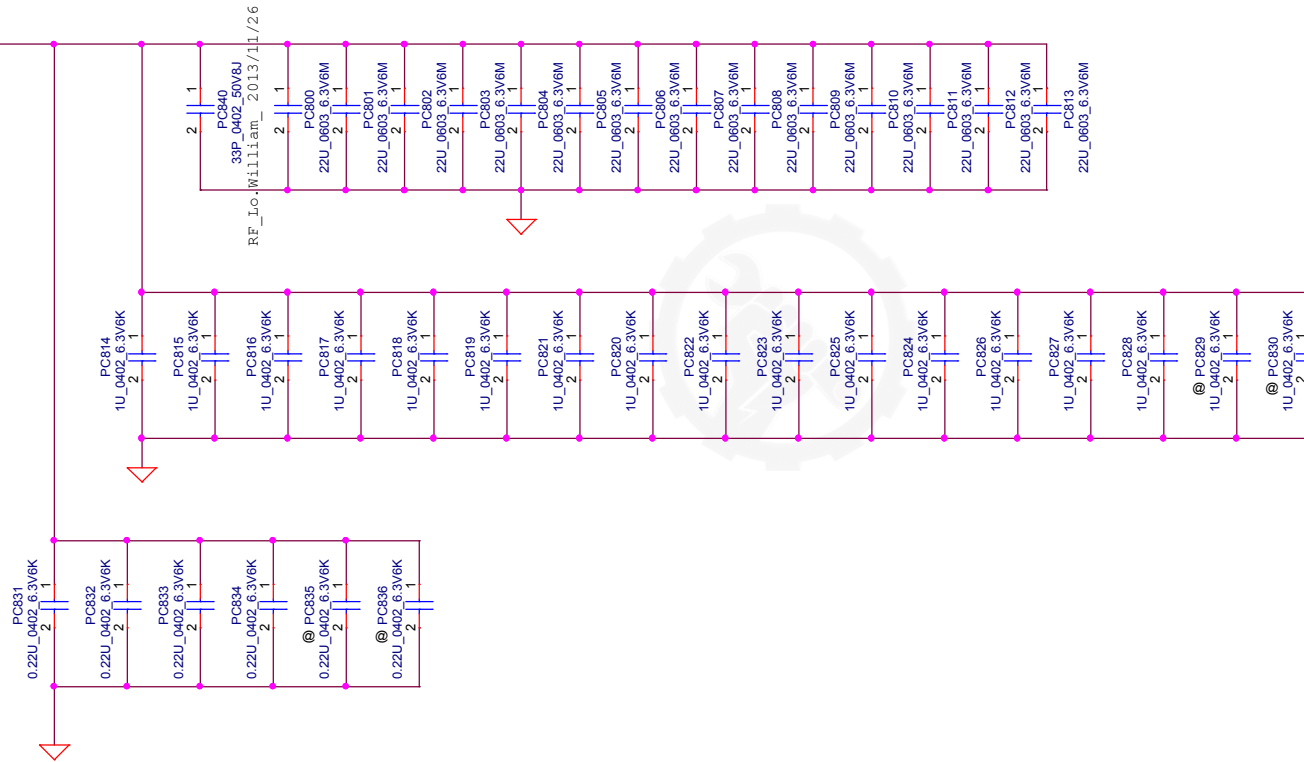


CPU_Core output CAP(36.4)

10U X 15
47U X 4
33P X 1

for VCORE:1 phase ----> 20pcs

+VCC_CORE



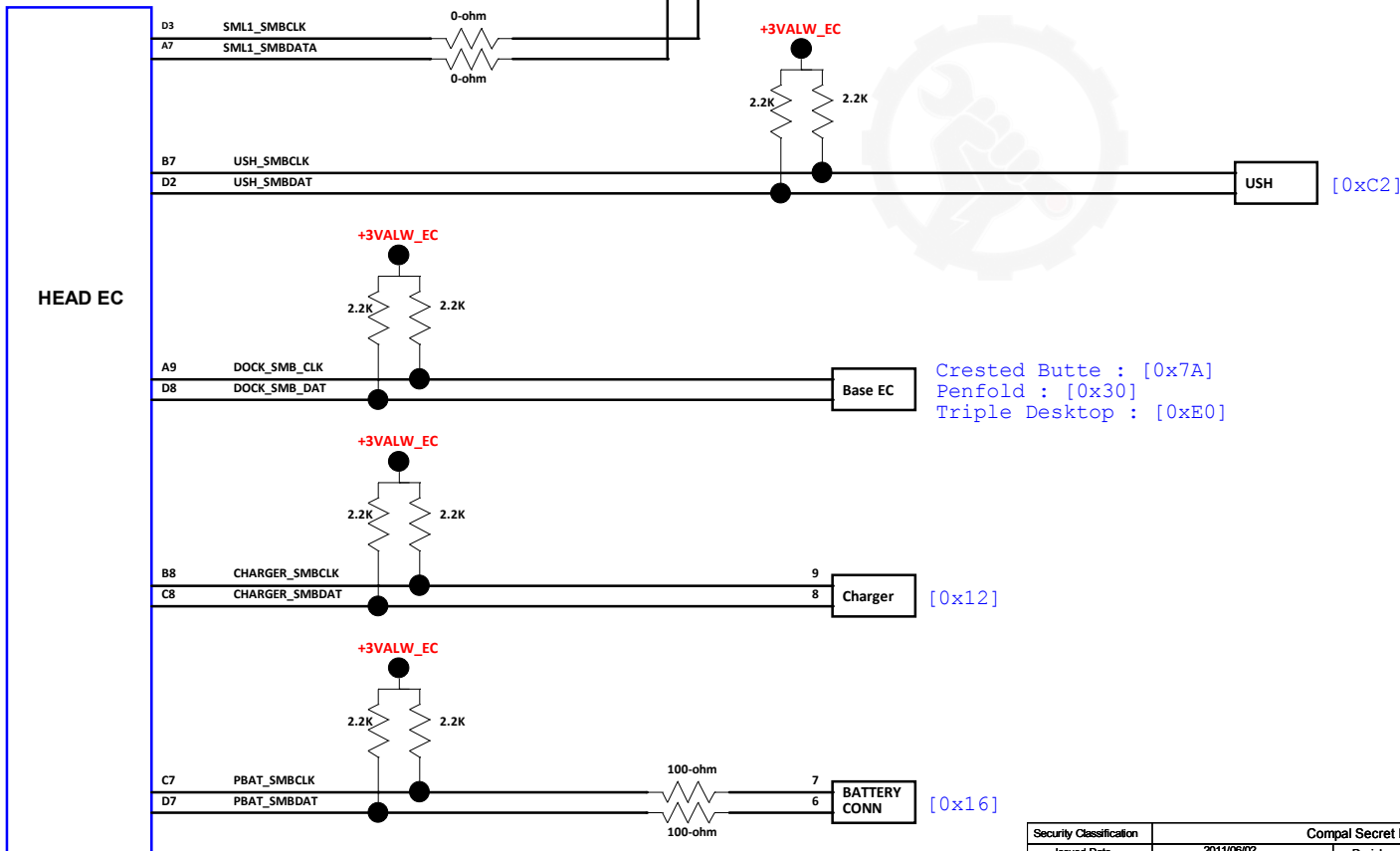
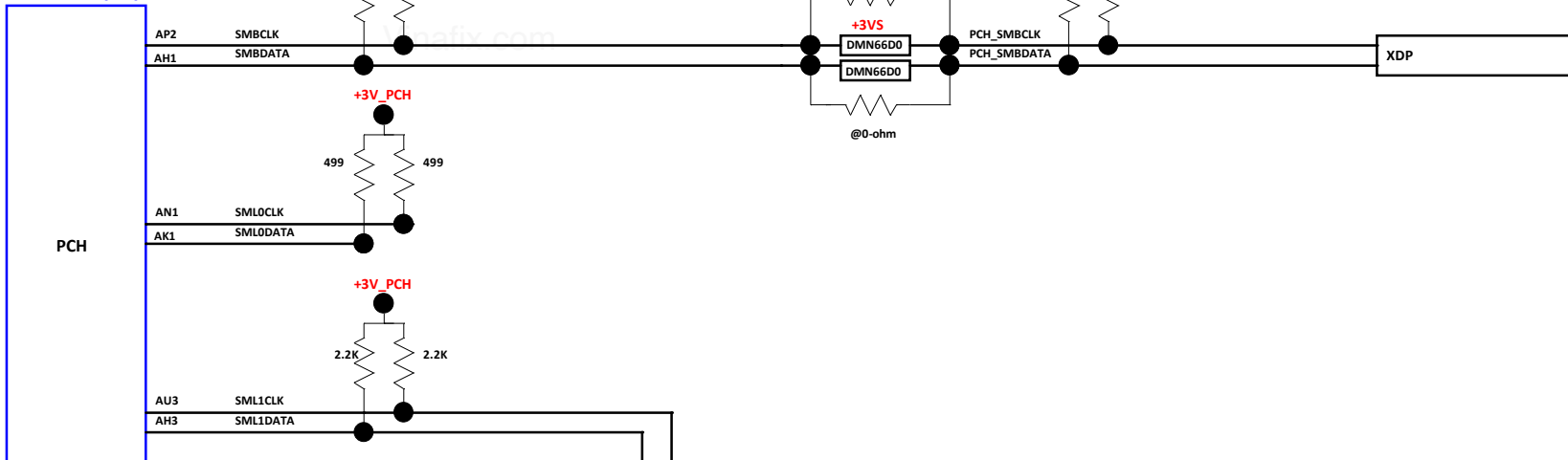
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P43-PWR PROCESSOR DECOUPLING
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Security Classification		Compal Secret Data		Compal Electronics, Inc. P44-PWR PIR-1	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title P44-PWR PIR-1	
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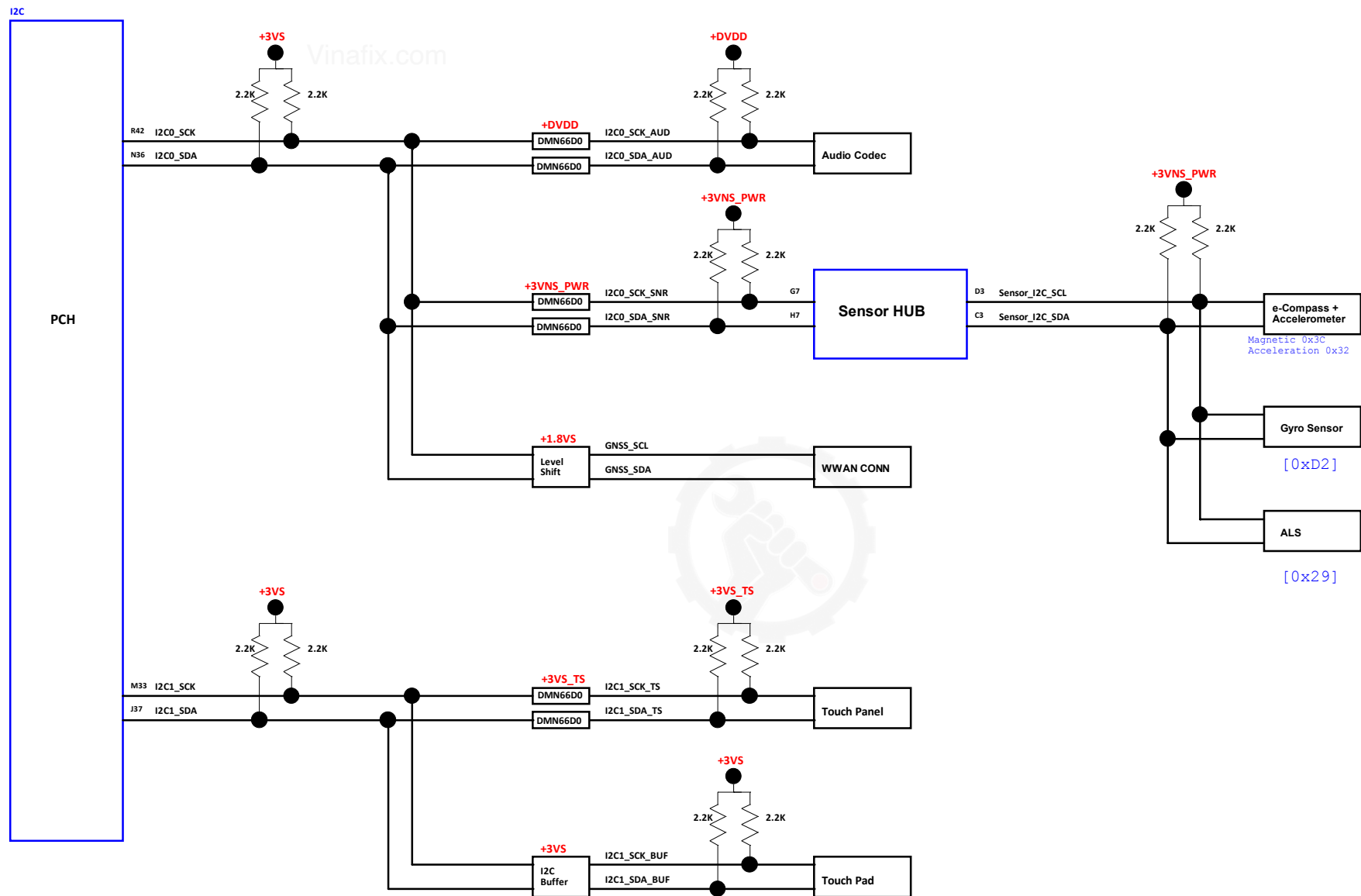
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title		
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					LA-9261P	0.1
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SMBUS Address [0x9a]



Crested Butte : [0x7A]
Penfold : [0x30]
Triple Desktop : [0xE0]

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P42-SMBus Block Diagram
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Discrete Power On Sequence

EC pay attention timing

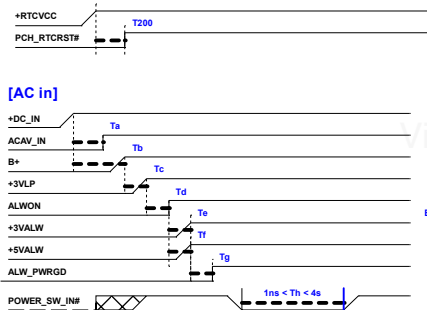
[AC in]

[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	+DC_IN	To
Tb	+DC_IN	To
Tc	B+	To
Td	+3VLP	To
Te	ALWON	To
Tf	ALWON	To
Tg	+5VALW	To
Th	POWER_SW_#	To
		Low pulse width

ITEM	Measure Point	Time
Ta	+DC_IN	To
Tb	B+	To
Tc	+3VLP	To
Th	POWER_SW_#	To
	Low pulse width	
Td	POWER_SW_#	To
Te	ALWON	To
Tf	ALWON	To
Tg	+5VALW	To
Tg	ALW_PWRGD	To

ITEM	Measure Point	Time
T1	PCH_ALW_ON	To
T2	PCH_ALW_ON	To
T3	PCH_RSMRST#	To
T4	PCH_RSMRST#	To
T5	PCH_RSMRST#	To
T6	PCH_ALW_ON	To
T7	SIO_SLP_WLAN#	To
T8	PCH_RSMRST#	To
T9	SIO_SLP_M#	To
T10	A_ON	To
T11	A_ON	To
T12	+3.3V_M	To
T13	SIO_PWRBTN#	To
T14	SIO_SLP_S#	To
T15	SIO_SLP_S#	To
T16	SUS_ON	To
T17	SIO_SLP_S#	To
T18	SIO_SLP_S#	To
T19	RUN_ON	To
T20	RUN_ON	To
T21	RUN_ON	To
T22	RUN_ON	To
T23	RUN_ON	To
T24	+5VS	To
T25	RUNPWROK	To
T26	SIO_SLP_S#	To
T27	MPHY_PWREN	To
T28	SIO_SLP_S#	To
T29	SATAMPHY_PWREN	To
T30	SIO_SLP_S#	To
T31	USB3MPHY_PWREN	To
T32	RESET_OUT#	To
T33	SM_PG_CTRL	To
T34	RESET_OUT#	To
T35	VR12.6_VR_ON	To
T36	+VCC_CORE	To
T37	VGATE	To
T38	VGATE	To
T39	SUS_ON	To
T40	To	
T41	To	
T42	To	



[Battery only, AC absent]

